

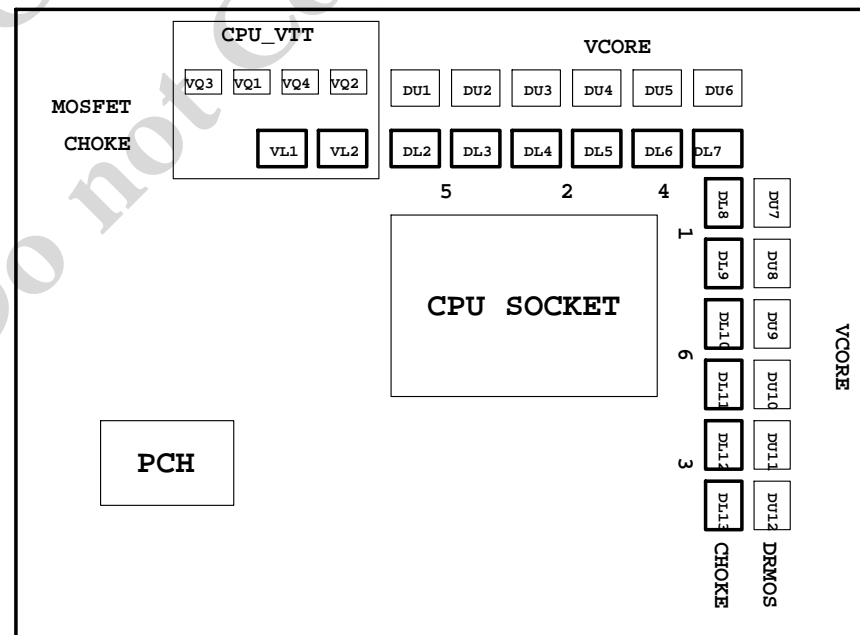
Model Name: GA-Z68XP-UD3P

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTS X3
18	IT8892
19	PCI SLOT 1&2
20	I/O ITE8728
21	COM, -PROHOT, ESATA CONNECT
22	Dual BIOS , TPM SLB9635TT
23	ALC899
24	REAR AUDIO JACK
25	VCORE PWM_ISL6366CRZ-1
26	VCORE PWM_ISL6366CRZ-2
27	VCORE PWM_ISL6366CRZ-3
28	N/A

29	DISCRETE POWER I
30	DDR_15V & VCC1_05_PCH PWM_ISL6545CBZ
31	CPU_VTT PWM_ISL6322G
32	VCCSA POWER
33	F_PANEL , F_USB , FDD
34	ATX POWER, CLOCK GEN
35	HWM,KB/MS , FAN CTRL
36	REALTEK RTL8111E
37	VT6308P 1394
38	REAR ET168A USB3.0
39	FRONT EJ168A USB3.0
40	MARVELL 9172
41	N/A
40	TABLE LIST



Gigabyte Technology

Title		Cover Sheet	
Size	Document Number	Rev	
Custom	GA-Z68XP-UD3P	1.3	
Date:	Tuesday, July 19, 2011	Sheet	1 of 44

GA-Z68X-UD3P
Component value change history

www.xinxunwei.com 400-800-9990

Data	Change Item	Reason
2011/02/21	9MP6XU3PB-00-01	P67X-UD3P-B3-01_20110221_1000_BOM.DSN
	EVT RELEASE	
2011/03/24	9MZ68XU3P-00-10A	
更換	MR23,316/4/1變更爲330/4/1	
	DR172,DR172,150K/4變更爲330K/4/1	
	DR168,VR52,1K/4/1變更爲499/4/1	
	DR220,25.5K/4/1變更爲40.2K/4/1	
	DR263,100K/4/1變更爲162K/4/1	
	DR259,200K/4/1變更爲324K/4/1	
	NR17,40.2K/4/1變更爲10K/4/1	
	R16,40.2K/4/1變更爲20K/4/1	
	MR22,NR197,20K/4/1變更爲4.99K/4/1	
	GSATA3_6_7,SATA/14/BK/H/OP/RA/D/2變更爲'SATA/14/GR/H/OP/RA/D/2	
	PCH,BD82P67/B3/S變更爲BD82Z68/B3/S	
	R24,12K/4/1變更爲8.2K/4/1	
	UAFB1,UAFB2,UBF1,UBF2,SMD1206P300SLR/S變更爲SMD1812P350SLR/S/[10FP1-06350B-20R]	
	DR199,54.9K/4/1變更爲110K/4/1	
	DR262,49.9K/4/1變更爲80.6K/4/1	
	DR182,165K/4/1變更爲330K/4/1	
	VU1,ISL6322G/QFN48/[10TA1-606322-21R]變更爲ISL6322G/QFN48/[10TA1-606322-11R]	
	DR139,47K/4/1變更爲8.2K/4/1	
	MR10,MR11,MR12,MR13,MR15,MR16,MR4,MR5,MR6,MR7,499/4/1變更爲1K/4/1	
	UBC6,UBC7,1u/4/X5R/6.3V/K變更爲0.1u/4/X7R/16V/K	
	DR14,DR133,DR15,DR16,DR102,DR114,DR138,DR7,DR61,DR40,DR31,DR56,332/4/1變更爲475/4/1	
	DR202,DR196,5.49K/4/1變更爲10K/4/1	
增加	C16,1u/4/X5R/6.3V/K R66,R75,270K/4 OR7,R106,R112,8.2K/4 IBC14,C25,DC142,DC143,DC505,DC506,0.1u/4/X7R/16V/K R108,R111,220/6 Q28,Q33,Q40,2N7002/SOT23/25pF/5 DC504,22u/8/X5R/6.3V/M Q35,Q39,PMBT2907A/SOT23/-600mA/50 AD1,AZ2225-01L/SOD323 Q29,Q36,MMBT2222A/SOT23/600mA/40 R77,R110,2K/4 C29,DC501,DC502,1u/6/X7R/16V/K RAEC1,100u/OS/D/16V/66/30m NX2-SHT,SHW/D0.64*5.08*6.74 R127,1K/4/1	刪除 R1,LAR3,LABC25,RBR20,LAR14,0/4 DBC102,0.1u/4/X7R/16V/K R48,OR12,OR15,DR349,DR339,DR317,R52,8.2K/4 R56,R57,220/6 CESD1,CESD2,CESD3,CESD4,CESD5,AZ2025-04S/SOT23-5L/[10TA1-012025-10R] NR28,33/4 Q27,DQ46,2N7002/SOT23/25pF/5 RABC21,22u/8/X5R/6.3V/M RARN1,0/8P4R/4 Q15,DQ43,Q14,PMBT2907A/SOT23/-600mA/50 DQ48,Q16,Q17,MMBT2222A/SOT23/600mA/40 R49,R51,R53,22K/4 NX3-SHT,SHW/D0.64*5.08*6.74 DR343,DR295,75K/4/1 DR320,DR344,DR326,1K/4/1

Circuit or PCB layout change

DATE	Change Item	Reason
2011/02/18	Change from P67X-UD4-B3 Rev0.1	P67X-UD3P-B3-01_20110218_1000.DSN
Rev:0.1		
2011/03/09	Remove LAR11,LAR14,NR28	P67X-UD3P-B3-10A_20110308_1800.DSN
REV1.0	NX3-SHT --> NX2-SHT	
	CR44 --> R0603-RH	
	CESD1,CESD2,CESD3,CESD4,CESD5 --> SSOP5	
	CESD2標示PIN1	
	Add DR388,DR389,DR391	
	Remove DR371,DQ49,DR347	
	R1,LABC25,LAR3,RBR20 --> R0402-2-SHORT10-MASK	
	Remove LAR11,LAR14	
	Remove IU2	
	RAQ1 --> Q_TO223-MASK	
	RARN1 --> R8P4R-0402-SHORT	
	RAQ2,RAEC1下移40MIL	
2011/03/21	Model name change to GA-Z68X-UD3P-B3	
REV1.0	USB3.0 Fuse change to 1812 3.5A	
	CEC1-CEC10;RAEC1;UBEC2 change to EC6D8MM-RH-1	
	Add DC500,DC501,DC502,DC504,DC505,DC506,DC142,DC143	
	Add R130	
2011/03/24	9MZ68XU3P-00-10B	2011/03/30 9MZ68XU3P-00-10C
	1.PCIE 36P 改爲11AC1-021036-B1R	1.Add C23,0.1u/4/X7R/16V/K
	2.MOS Heatsink改爲用料一	2.Add C24,1u/4/X5R/6.3V/K
	2011/03/24 9MZ68XU3P-00-10D	
	1.C14-->0.1u/6	
	2.R95-->22K/4	
	2011/07/19	
	1.PCB 改文字面版本爲1.3	

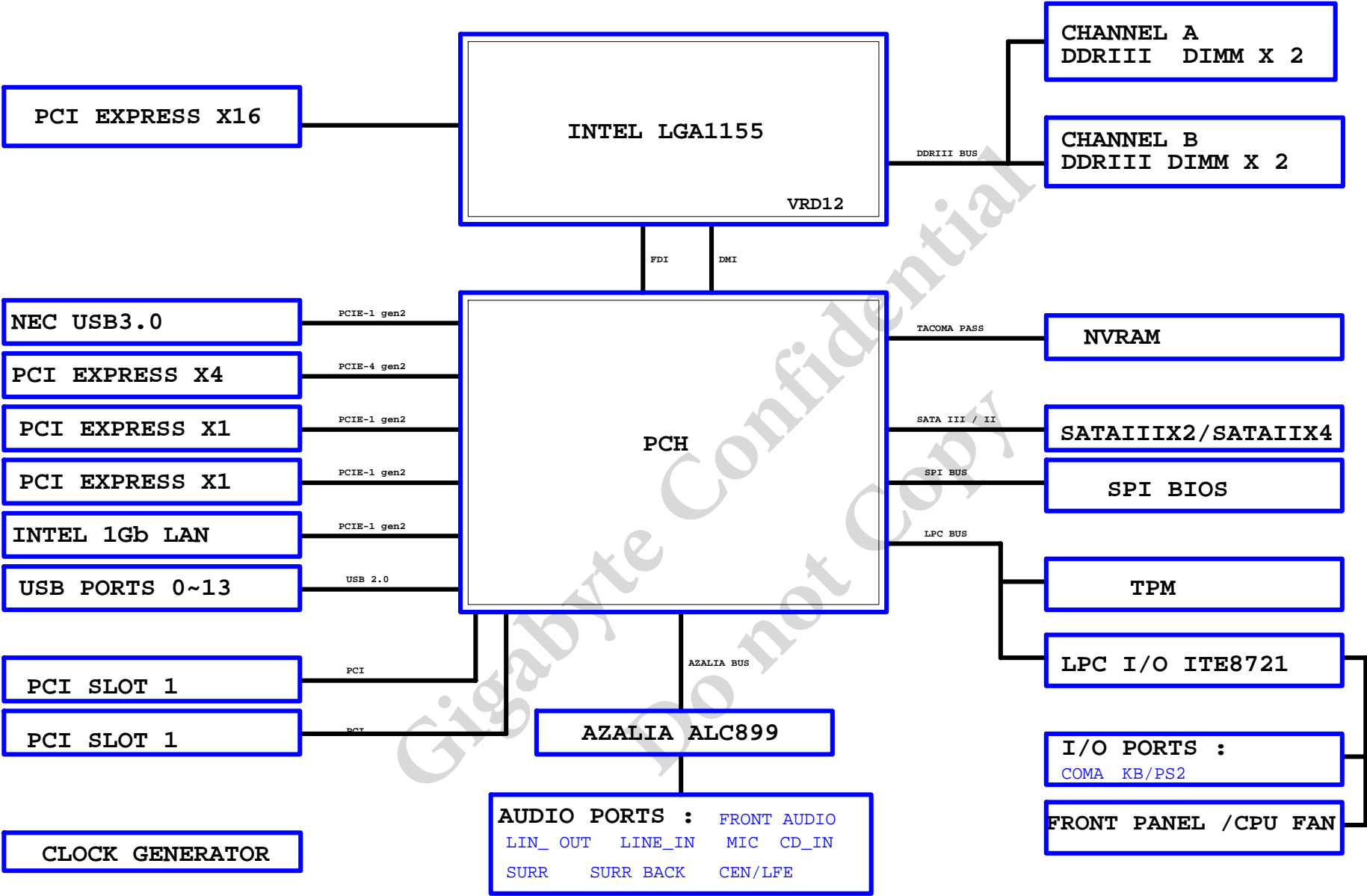
2.文字面Dual PCI Express 2.0 ==>Dual PCI Express 3.0

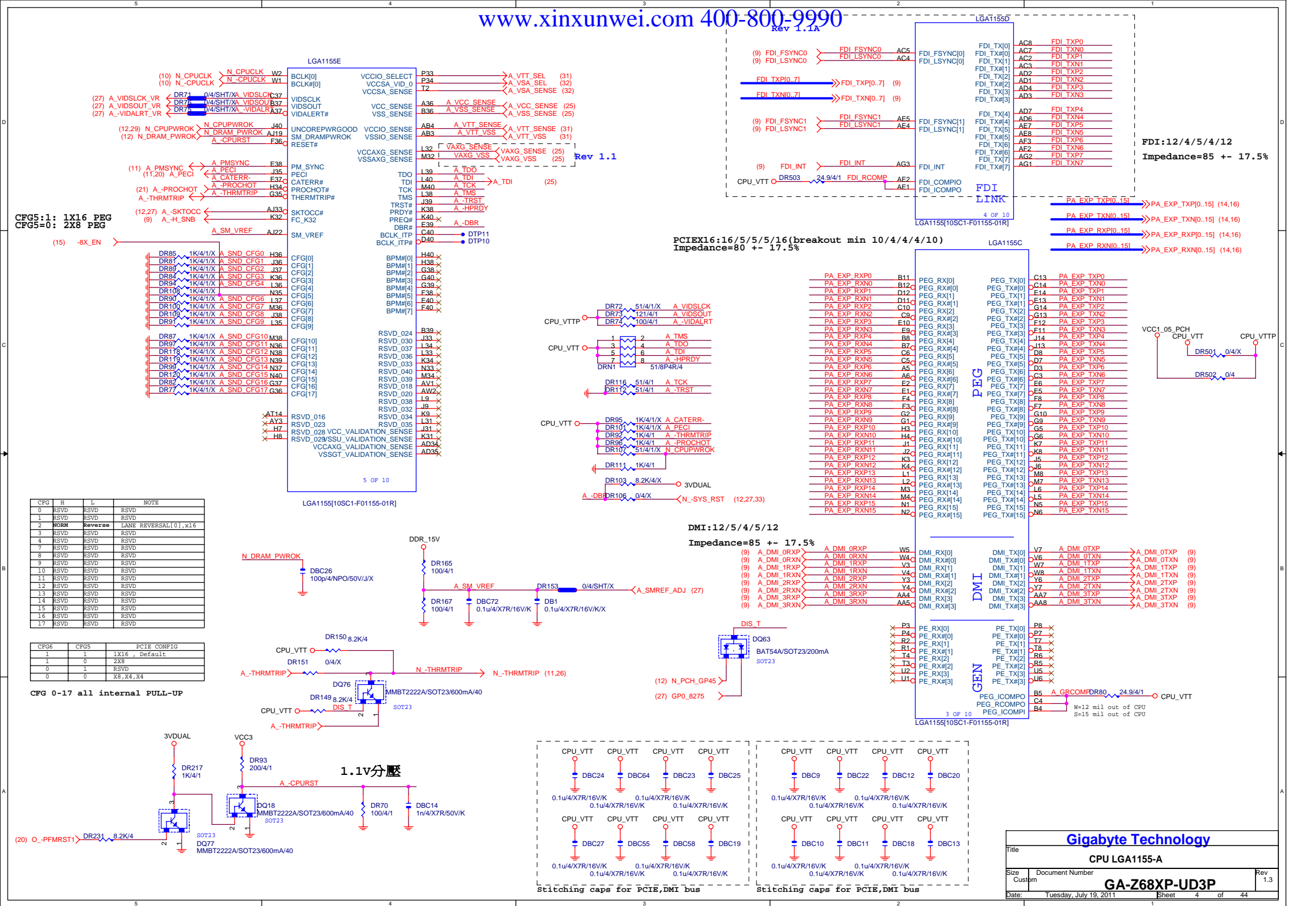
2011/07/19 9MZ68XU3P-00-13A

1.PI3PCIE2415ZHE/TQFN42==>PI3PCIE3415ZHE/TQFN42/[10TA1-083415-10R]

Gigabyte Technology		
BOM & PCB MODIFY HISTORY		
Title	Document Number	
Size	GA-Z68X-UD3P	
Custom	Rev	
Date:	Tuesday, July 19, 2011	1.3
	Sheet	2 of 44

BLOCK DIAGRAM





LGA1155A

M_AAA0	AV27	SA_MA[0]
M_AAA1	AY24	SA_MA[1]
M_AAA2	AW24	SA_MA[2]
M_AAA3	AV23	SA_MA[3]
M_AAA4	AV23	SA_MA[4]
M_AAA5	AT24	SA_MA[5]
M_AAA6	AT23	SA_MA[6]
M_AAA7	AU22	SA_MA[7]
M_AAA8	AV22	SA_MA[8]
M_AAA9	AT22	SA_MA[9]
M_AAA10	AV28	SA_MA[10]
M_AAA11	AU21	SA_MA[11]
M_AAA12	AU21	SA_MA[12]
M_AAA13	AU32	SA_MA[13]
M_AAA14	AU20	SA_MA[14]
M_AAA15	AT20	SA_MA[15]

(7) M_SWEA	M_SWEA	AW29	SA_WE#
(7) M_SCASA	M_SCASA	AV30	SA_CAS#
(7) M_SRASA	M_SRASA	AU28	SA_RAS#

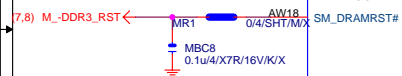
(7) M_SBA0	M_SBA0	AY29	SA_BS[0]
(7) M_SBA1	M_SBA1	AW28	SA_BS[1]
(7) M_SBA2	M_SBA2	AV20	SA_BS[2]

(7) M-CSA0	M-CSA0	AU29	SA_CS#0]
(7) M-CSA1	M-CSA1	AV32	SA_CS#1]
(7) M-CSA2	M-CSA2	AW30	SA_CS#2]
(7) M-CSA3	M-CSA3	AU33	SA_CS#3]

(7) M_CKEA0	M_CKEA0	AV19	SA_CKE[0]
(7) M_CKEA1	M_CKEA1	AT19	SA_CKE[1]
(7) M_CKEA2	M_CKEA2	AU18	SA_CKE[2]
(7) M_CKEA3	M_CKEA3	AV18	SA_CKE[3]

M_ODT_A0	AV31	SA_ODT[0]
M_ODT_A1	AU32	SA_ODT[1]
M_ODT_A2	AU30	SA_ODT[2]
M_ODT_A3	AW33	SA_ODT[3]

(7) M_DCLKA0	M_DCLKA0	AY25	SA_CK[0]
(7) M_DCLKA1	M_DCLKA1	AW25	SA_CK#0]
(7) M_DCLKA1	M_DCLKA1	AU24	SA_CK[1]
(7) M_DCLKA2	M_DCLKA2	AU25	SA_CK#1]
(7) M_DCLKA2	M_DCLKA2	AY27	SA_CK[2]
(7) M_DCLKA3	M_DCLKA3	AV26	SA_CK#2]
(7) M_DCLKA3	M_DCLKA3	AW26	SA_CK[3]



AV13	SA_DQS[8]
AV12	SA_DQS#8]
AU12	SA_ECC_CB[0]
AU14	SA_ECC_CB[1]
AW13	SA_ECC_CB[2]
AY13	SA_ECC_CB[3]
AU13	SA_ECC_CB[4]
AY12	SA_ECC_CB[5]
AW12	SA_ECC_CB[7]

DDR_0

1 OF 10

LGA1155[10SC1-F01155-01R]

AK3	M_DQSA0
AK2	M_DQSA0
AJ3	M_DA0
AJ4	M_DA1
AL3	M_DA2
AL4	M_DA3
AJ2	M_DA4
AJ1	M_DA5
AL2	M_DA6
AL1	M_DA7

AP3	M_DQSA1
AP2	M_DQSA1

AN1	M_DA8
AN4	M_DA9
AR3	M_DA10
AR4	M_DA11
AN2	M_DA12
AN3	M_DA13
AR2	M_DA14
AR1	M_DA15

AW4	M_DQSA2
AW4	M_DQSA2

AV2	M_DA16
AW3	M_DA17
AV5	M_DA18
AW5	M_DA19
AU2	M_DA20

AU3	M_DA21
AU5	M_DA22
AY5	M_DA23

AV8	M_DQSA3
AW8	M_DQSA3

AY7	M_DA24
AU7	M_DA25
AV9	M_DA26
AU9	M_DA27
AV7	M_DA28
AW7	M_DA29
AW9	M_DA30
AY9	M_DA31

AV37	M_DQSA4
AV36	M_DQSA4

AU35	M_DA32
AW37	M_DA33
AU38	M_DA34
AU36	M_DA35
AW35	M_DA36
AY36	M_DA37
AU38	M_DA38
AU37	M_DA39

AP38	M_DQSA5
AP39	M_DQSA5

AR40	M_DA40
AR37	M_DA41
AN38	M_DA42
AN37	M_DA43
AR39	M_DA44
AR38	M_DA45
AN38	M_DA46
AN40	M_DA47

AK38	M_DQSA6
AK39	M_DQSA6

AL40	M_DA48
AL37	M_DA49
AJ38	M_DA50
AJ37	M_DA51
AL39	M_DA52
AL38	M_DA53
AJ39	M_DA54
AJ40	M_DA55

AF38	M_DQSA7
AF39	M_DQSA7

AG40	M_DA56
AG37	M_DA57
AE38	M_DA58
AE37	M_DA59
AG39	M_DA60
AG38	M_DA61
AE39	M_DA62
AE40	M_DA63

(7) M_ODT_A[0..3] < M_ODT_A[0..3]

(8) M_ODT_B[0..3] < M_ODT_B[0..3]

(7) M_DA[0..63] < M_DA[0..63]

(8) M_DB[0..63] < M_DB[0..63]

(7) M_DQSA[0..7] < M_DQSA[0..7]

(7) M_DQSA[0..7] < M_DQSA[0..7]

(7) M_AA[0..15] < M_AA[0..15]

(8) M_AAB[0..15] < M_AAB[0..15]

(8) M_DQSB[0..7] < M_DQSB[0..7]

(8) M_DQSB[0..7] < M_DQSB[0..7]

LGA1155B

M_AAB0	AK24	SB_MA[0]
M_AAB1	AM20	SB_MA[1]
M_AAB2	AM19	SB_MA[2]
M_AAB3	AK18	SB_MA[3]
M_AAB4	AP19	SB_MA[4]
M_AAB5	AP18	SB_MA[5]
M_AAB6	AM18	SB_MA[6]
M_AAB7	AL18	SB_MA[7]
M_AAB8	AY17	SB_MA[8]
M_AAB9	AN13	SB_MA[9]
M_AAB10	AN23	SB_MA[10]
M_AAB11	AU17	SB_MA[11]
M_AAB12	AT18	SB_MA[12]
M_AAB13	AR26	SB_MA[13]
M_AAB14	AY16	SB_MA[14]
M_AAB15	AV16	SB_MA[15]

(8) M_SWEB	M_SWEB	AR25	SB_WE#
(8) M_SCASB	M_SCASB	AK25	SB_CAS#
(8) M_SRASB	M_SRASB	AP24	SB_RAS#

(8) M_SBA0	M_SBA0	AP23	SB_BS[0]
(8) M_SBA1	M_SBA1	AM22	SB_BS[1]
(8) M_SBA2	M_SBA2	AW17	SB_BS[2]

(8) M-CSB0	M-CSB0	AN25	SB_CS#0]
(8) M-CSB1	M-CSB1	AN26	SB_CS#1]
(8) M-CSB2	M-CSB2	AL25	SB_CS#2]
(8) M-CSB3	M-CSB3	AT26	SB_CS#3]

(8) M_CKEB0	M_CKEB0	AL18	SB_CKE[0]
(8) M_CKEB1	M_CKEB1	AY15	SB_CKE[1]
(8) M_CKEB2	M_CKEB2	AW15	SB_CKE[2]
(8) M_CKEB3	M_CKEB3	AV15	SB_CKE[3]

M_ODT_B0	AL26	SB_ODT[0]
M_ODT_B1	AM26	SB_ODT[1]
M_ODT_B2	AM26	SB_ODT[2]
M_ODT_B3	AK26	SB_ODT[3]

(8) M_DCLKB0	M_DCLKB0	AL21	SB_CK[0]
(8) M_DCLKB0	M_DCLKB0	AL22	SB_CK#0]
(8) M_DCLKB1	M_DCLKB1	AL20	SB_CK[1]
(8) M_DCLKB1	M_DCLKB1	AK20	SB_CK#1]
(8) M_DCLKB2	M_DCLKB2	AL23	SB_CK[2]
(8) M_DCLKB2	M_DCLKB2	AM22	SB_CK#2]
(8) M_DCLKB3	M_DCLKB3	AP21	SB_CK[3]
(8) M_DCLKB3	M_DCLKB3	AN21	SB_CK#3]

(8) M_VREF_DQB	AH1	FC_AH1
(7) M_VREF_DQA	AH4	FC_AH4

AN16	SB_DQS[8]
AN15	SB_DQS#8]

AL16	SB_ECC_CB[0]
AM16	SB_ECC_CB[1]
AP16	SB_ECC_CB[2]
AR16	SB_ECC_CB[3]
AL15	SB_ECC_CB[4]
AM15	SB_ECC_CB[5]
AP15	SB_ECC_CB[6]
AR15	SB_ECC_CB[7]

AP32	M_DB40
AP31	M_DB41
AP35	M_DB42
AP34	M_DB43
AR32	M_DB44
AR31	M_DB45
AR35	M_DB46
AR34	M_DB47

AL33	M_DQSB6
AM33	M_DQSB6

AM32	M_DB48
AM31	M_DB49
AL35	M_DB50
AL32	M_DB51
AM34	M_DB52
AL31	M_DB53
AM35	M_DB54
AL34	M_DB55

AG35	M_DQSB7
AG34	M_DQSB7

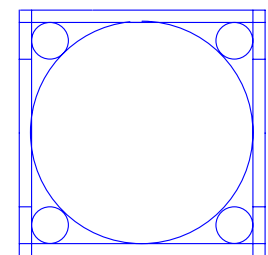
AH35	M_DB56
AH34	M_DB57
AE34	M_DB58
AE35	M_DB59
AJ35	M_DB60
AJ34	M_DB61
AF33	M_DB62
AF35	M_DB63

DDR_1

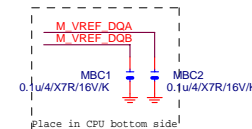
2 OF 10

LGA1155[10SC1-F01155-01R]

LGA1155



Need check the new CPU ME



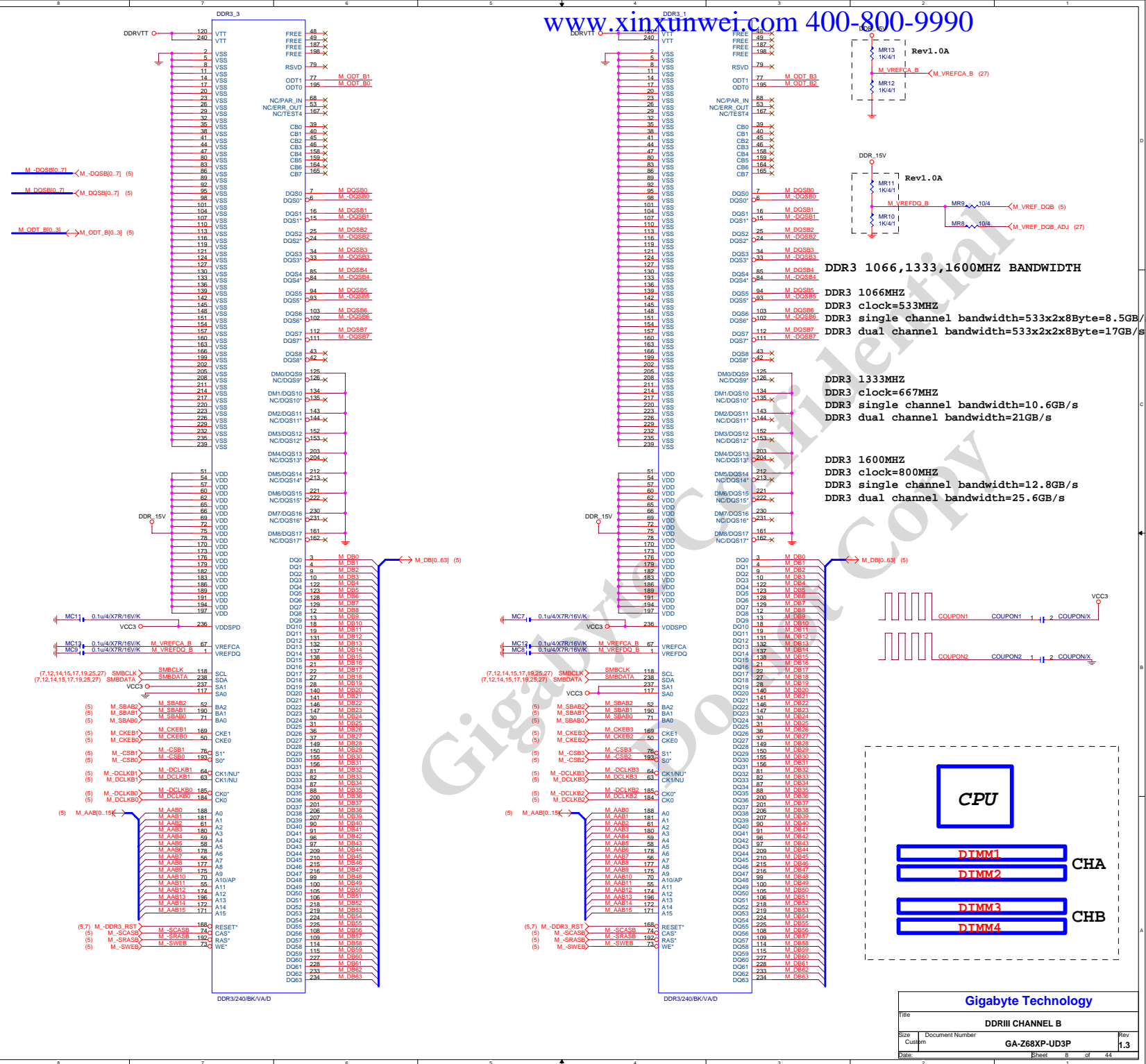
Place in CPU bottom side!

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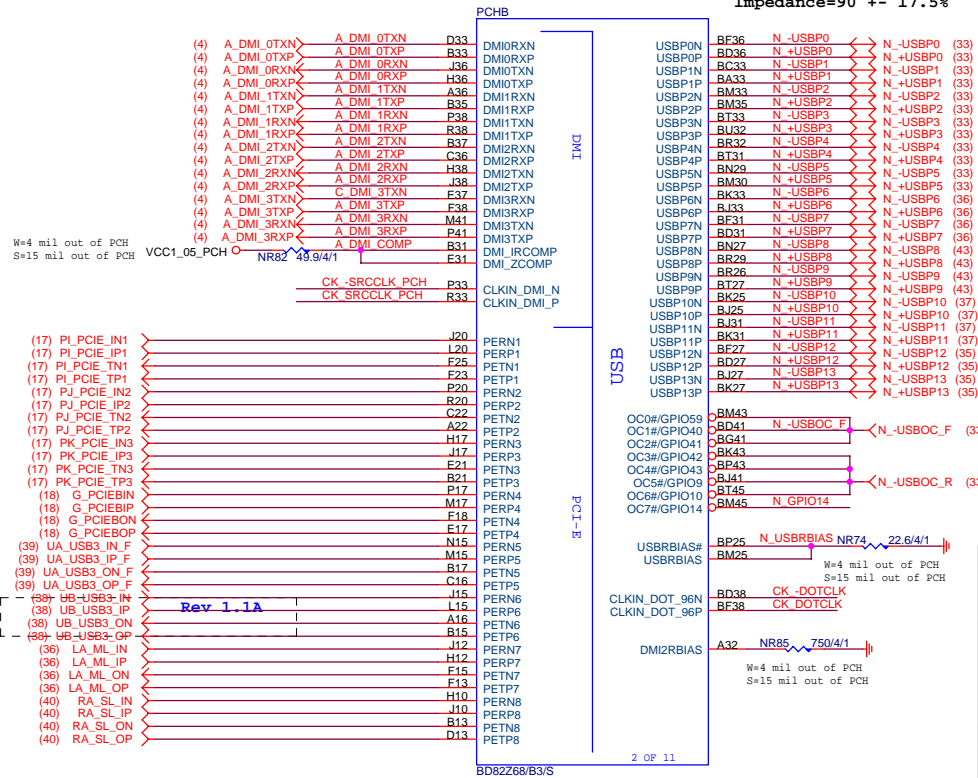
CPU LGA1156-B

Title	Document Number	Rev
Size	Custom	1.3
Date:	Tuesday, July 19, 2011	Sheet 5 of 44

GA-Z68XP-UD3P



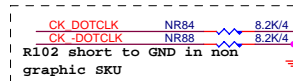
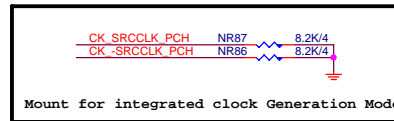
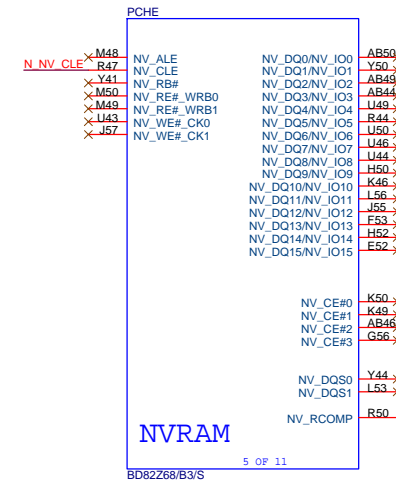
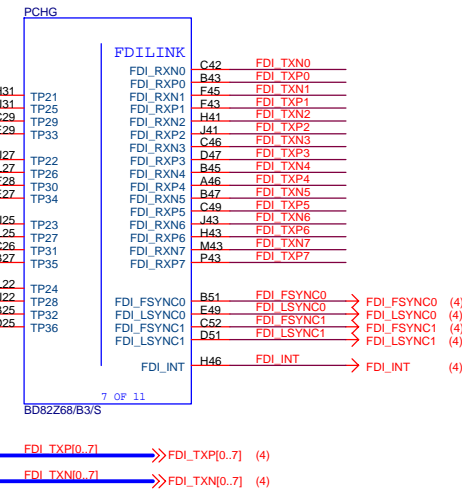
USB:12/7.5/4.5/7.5/12 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%



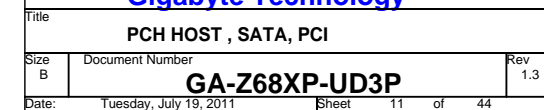
OC[3:0]# for
Device 29
(ports 0-7)

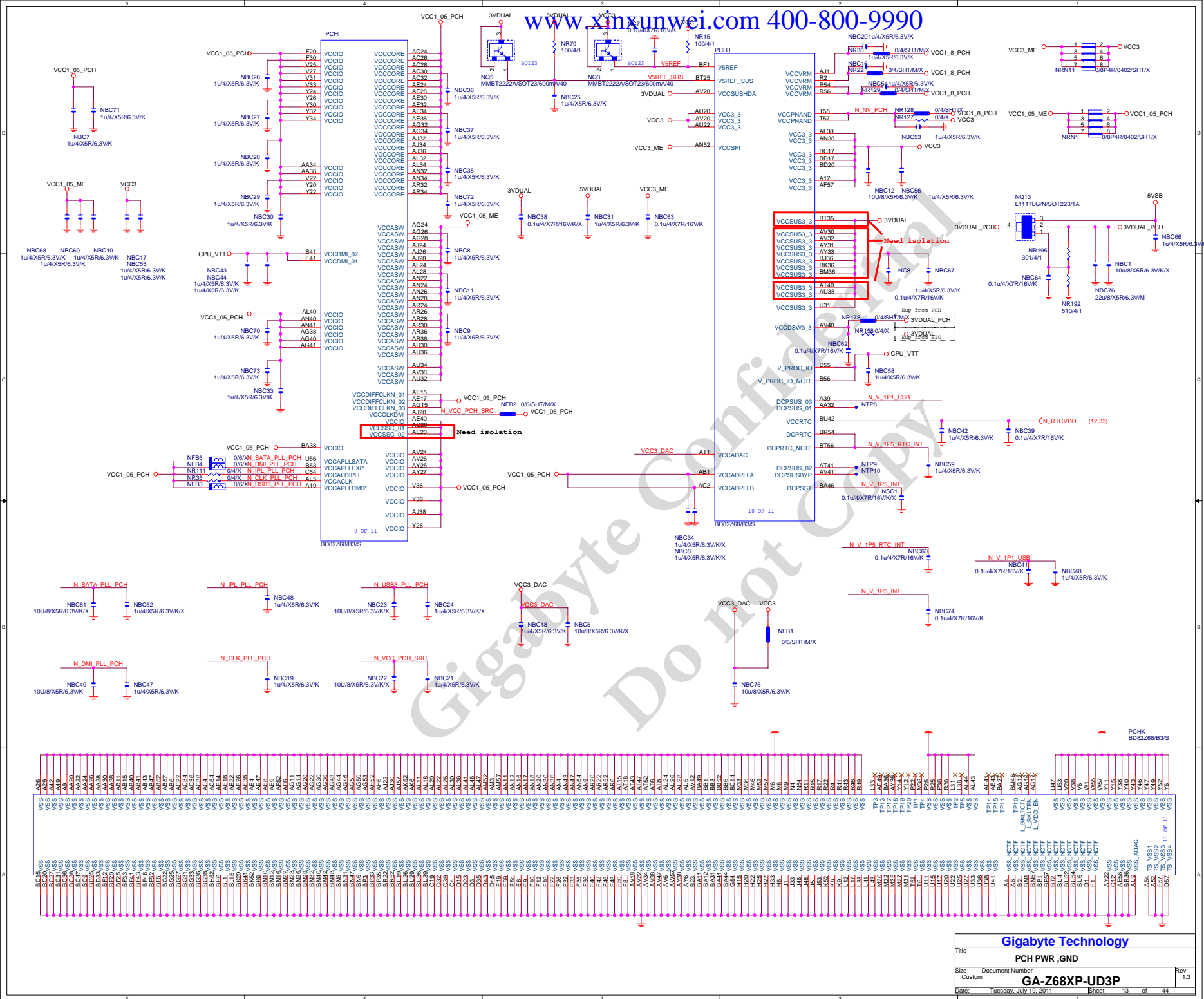
OC[7:4]# for
Device 26
(ports 8-13)

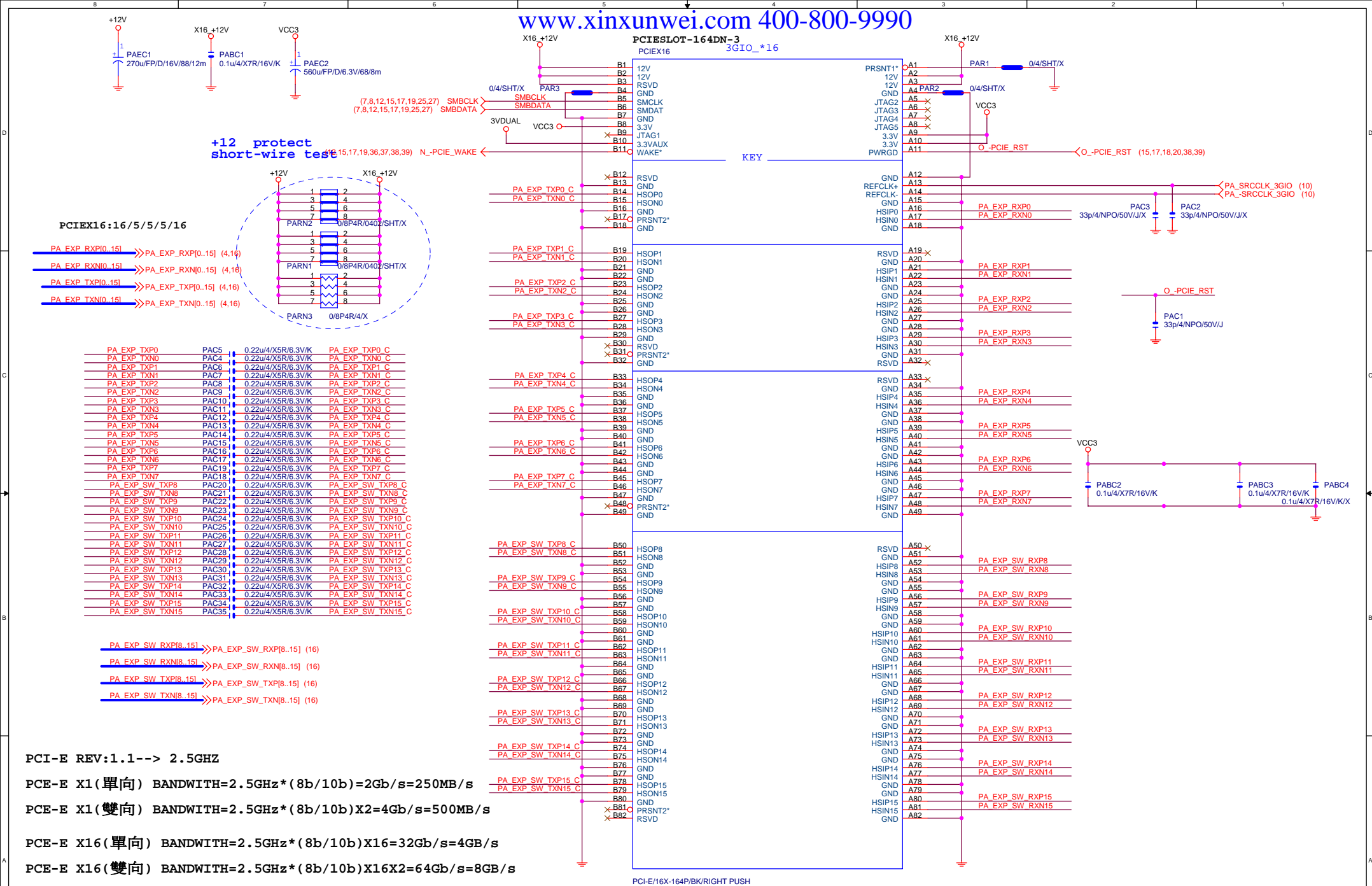
USB OC# Configure	
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use



Gigabyte Technology			
Title PCH DISPLAY ,CLK BUFFER			
Size	Document Number	Rev	
Custom	GA-Z68XP-UD3P	1.3	
Date:	Tuesday, July 19, 2011	Sheet	10 of 44

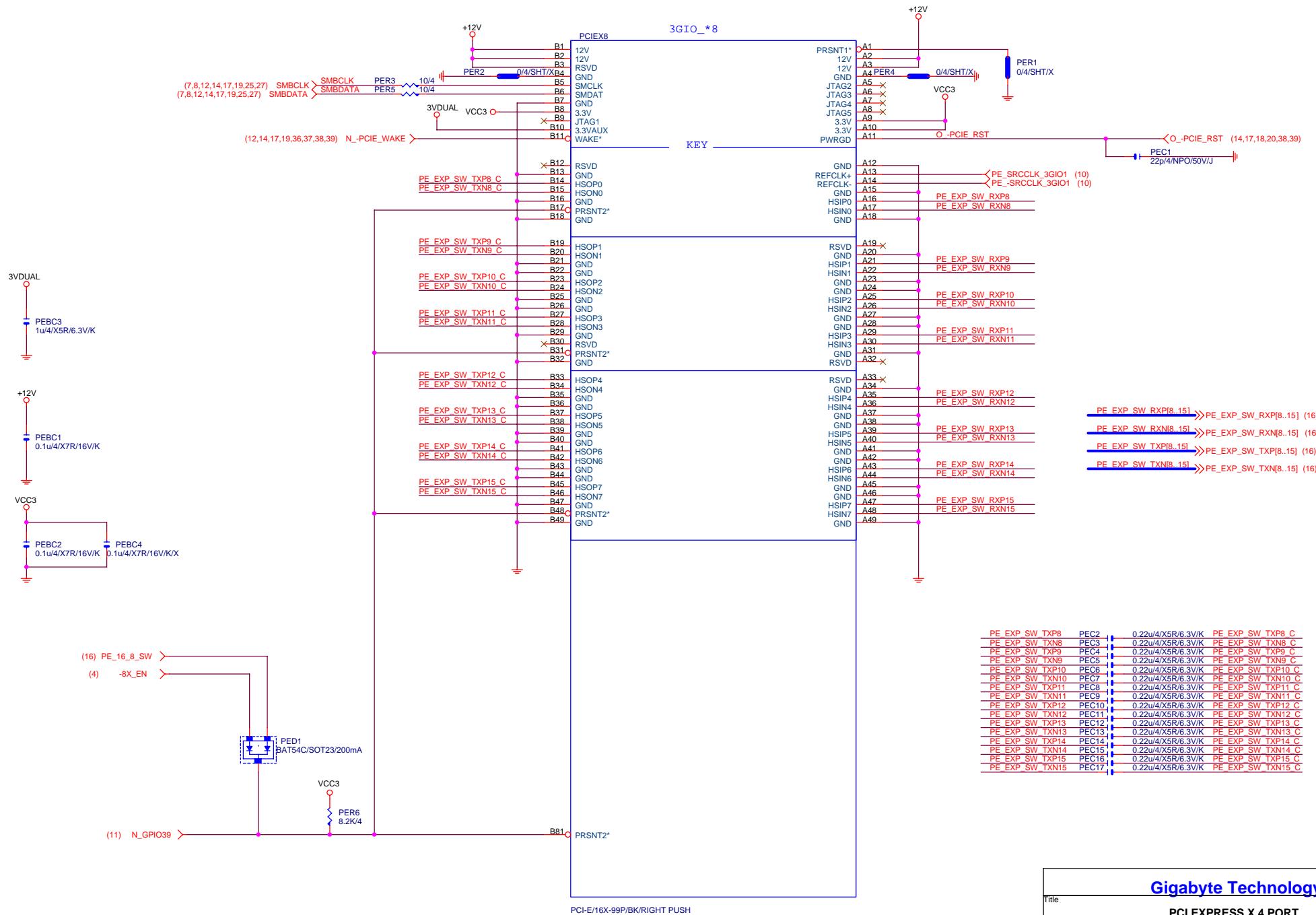






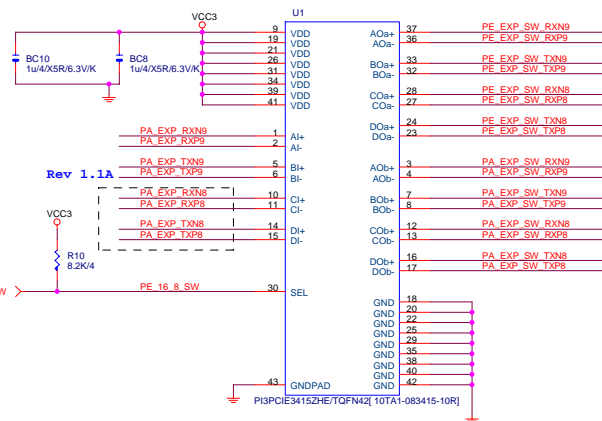
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Title			
PCI EXPRESS * 16			
Size	Document Number	Rev	
Custom	GA-Z68XP-UD3P	1.3	
Date:	Tuesday, July 19, 2011	Sheet	14 of 44

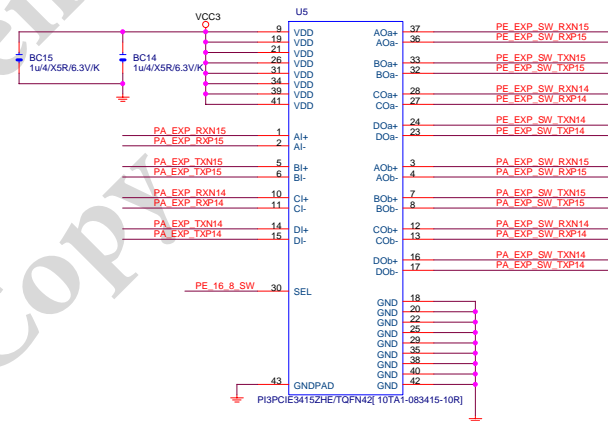
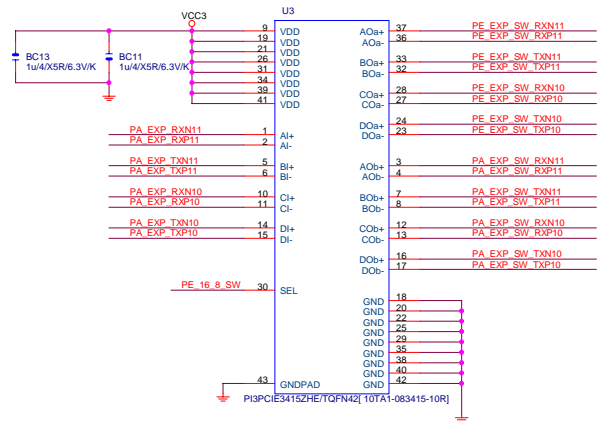
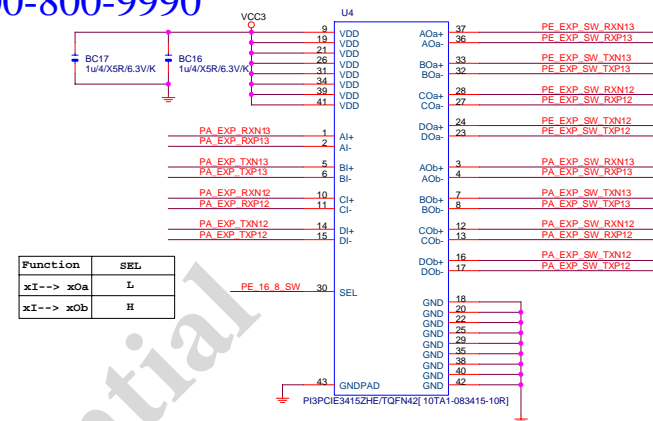


Gigabyte Technology

Title		
PCI EXPRESS X 4 PORT		
Size	Document Number	Rev
Custom	GA-Z68XP-UD3P	1.3
Date:	Tuesday, July 19, 2011	Sheet 15 of 44

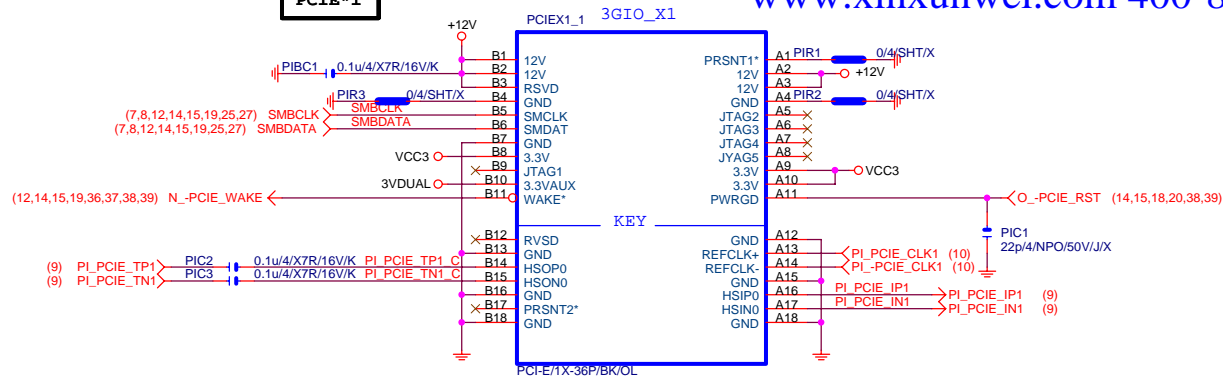


PI3PCIE3415ZHE/TQFN42[10TA1-083415-10R]

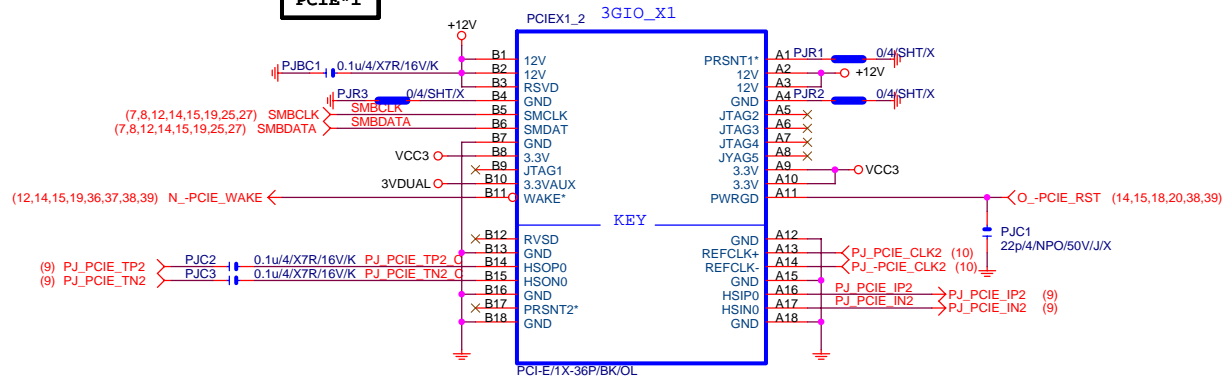


Rev 1.1A

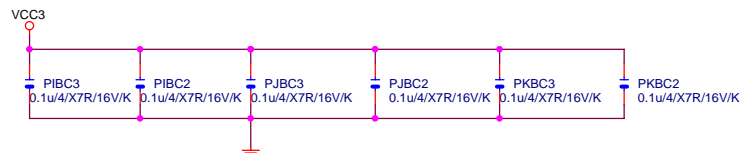
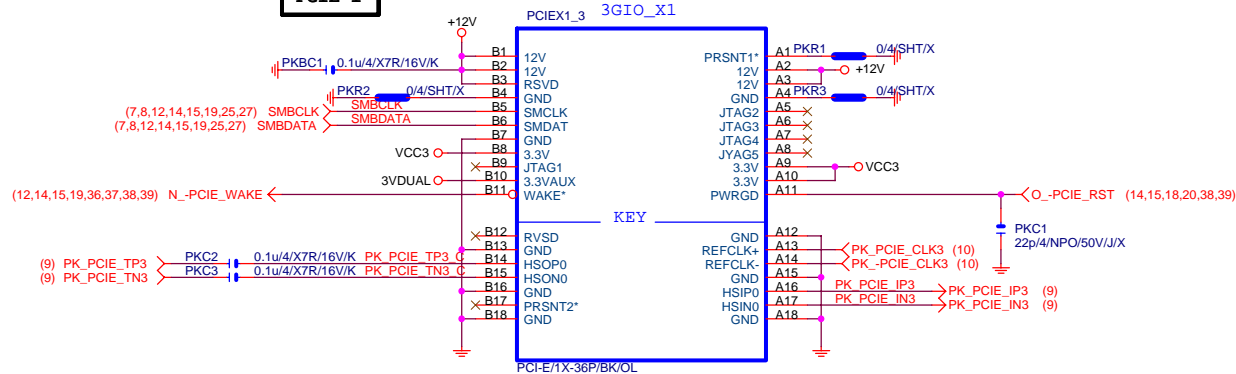
PCI-E*1



PCI-E*1

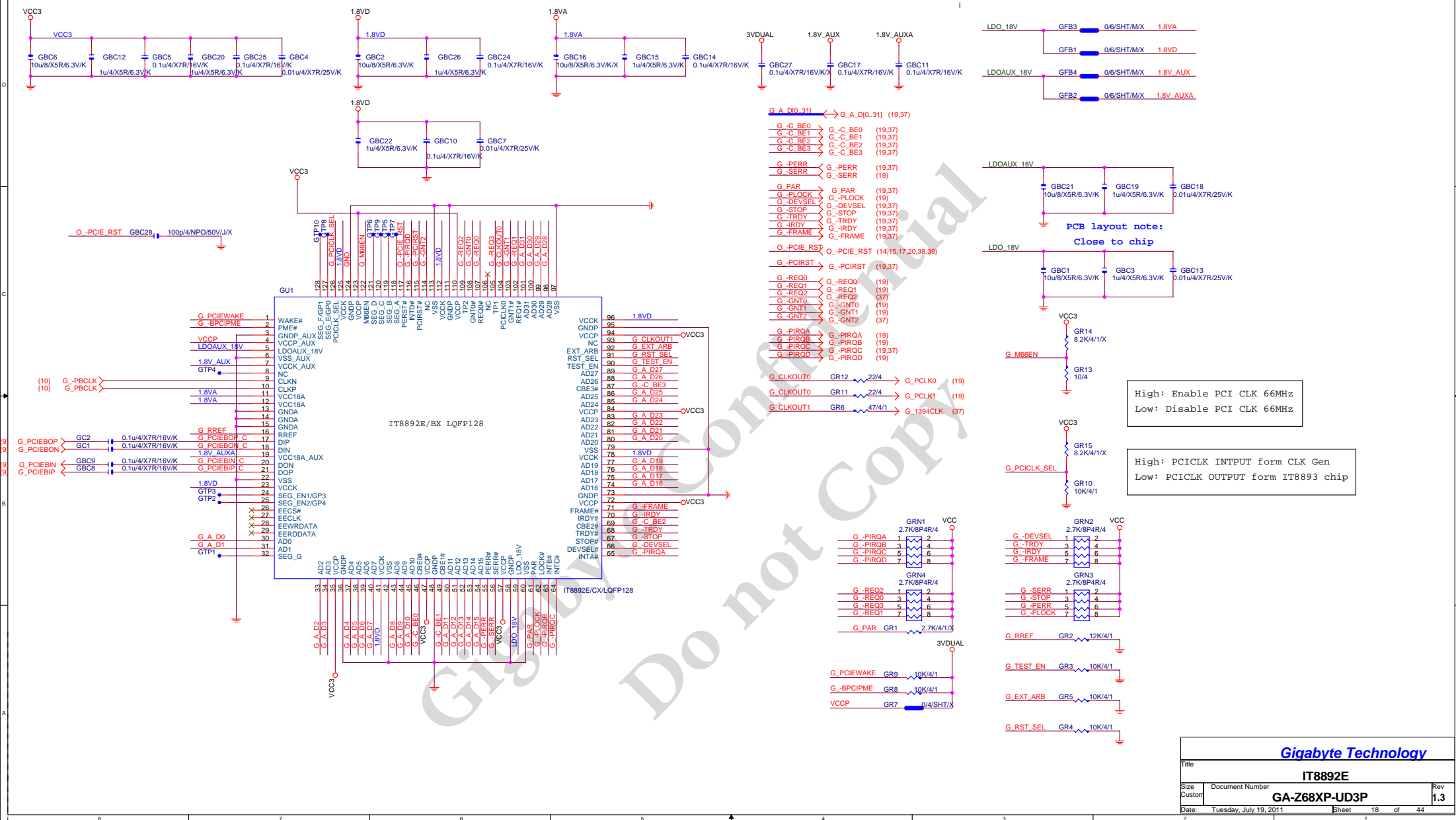


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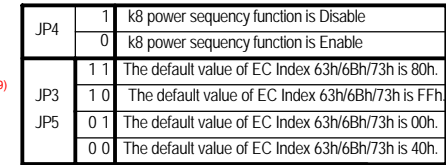


Gigabyte Technology

Title		
PCIE_X1 1,2		
Size	Document Number	Rev
Custom	GA-Z68XP-UD3P	1.3
Date:	Tuesday, July 19, 2011	Sheet 17 of 44

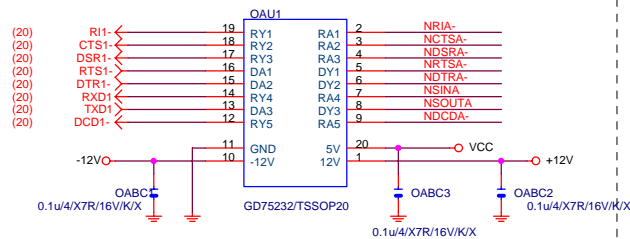




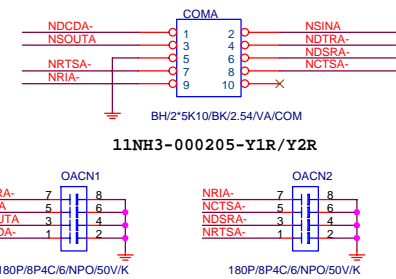
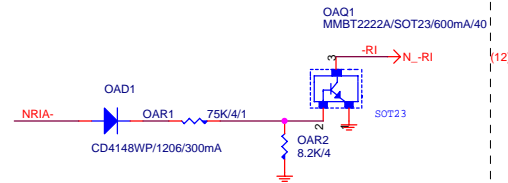


	IT8721	IT8728
PIN121	FAN_CTL4/VID_TURBO	VCORE_EN/PCH_C0
PIN120	VDDA_EN	VLDT_EN/PCH_D0
PIN19	GP30	ATXPG
PIN31	GP14	PCH_C1
PIN53	SST/AMDTSL_D/PECI_AVA/MTRB#/PCH_D	SST/AMDTSL_D/MTRB#/PCH_D1
PIN55	PECI/AMDTSL_C/DRV##/PCH_C	PECI/AMDTSL_C/DRV#
PIN66	GP47	SYS_3VSB
PIN70	SYS_3VSB	GP47
PIN95	VIN3/ATXPG	VIN2(VCC5)
PIN96	VIN2	VIN1(VCC12)
PIN97	VIN1(VCC5)	VIN1/VBIM_STR(1.5V)
PIN98	VIN0(VCC12)	VIN0/VCORE(1.1V)

COMA

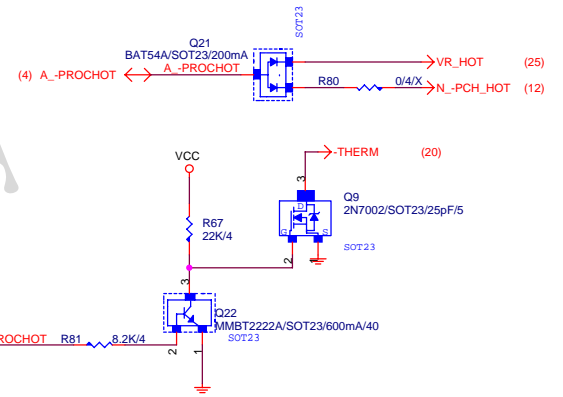


COM R1



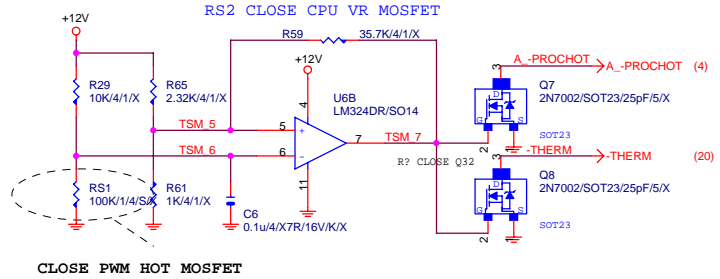
Rev1.1

Move to Page 43



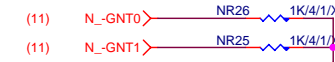
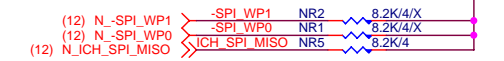
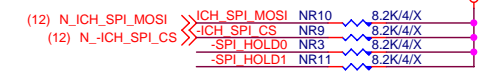
-PROHOT

deasserted at 116 degree



Gigabyte Technology

Title			COM & PROHOT/Dynamic O.C.	
Size	Document Number	GA-Z68XP-UD3P		Rev
Custom				1.3
Date:	Tuesday, July 19, 2011	Sheet	21	of 44



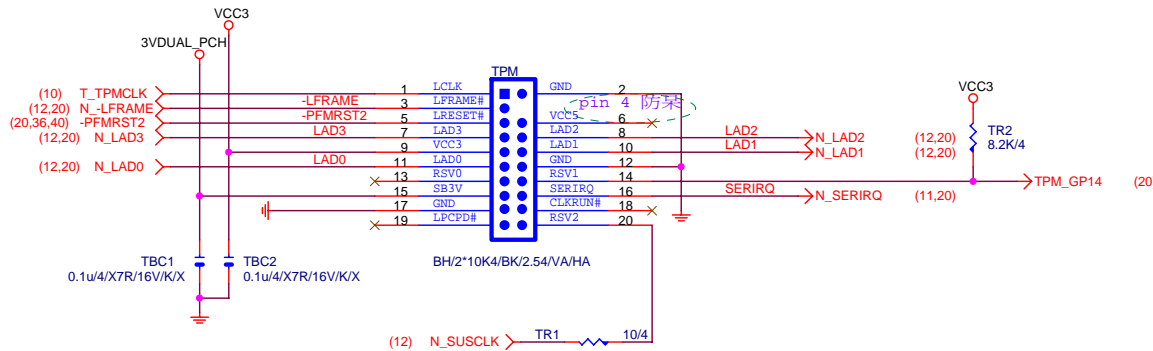
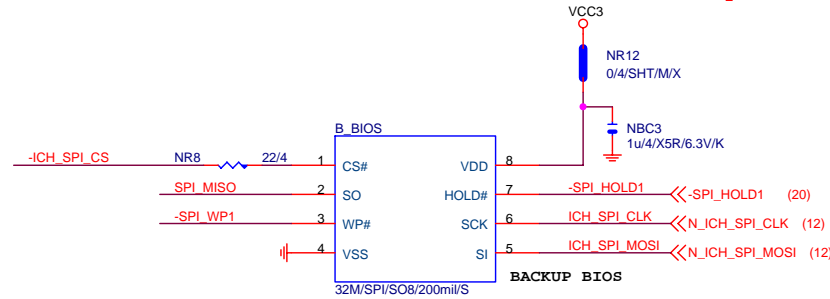
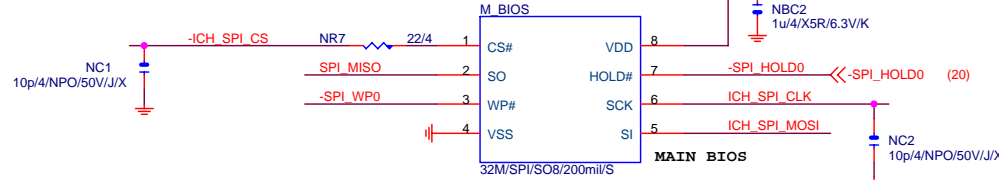
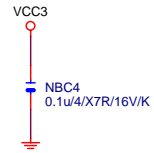
Default int pull up



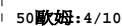
BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

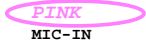
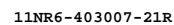
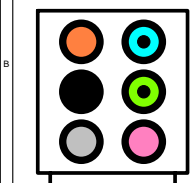
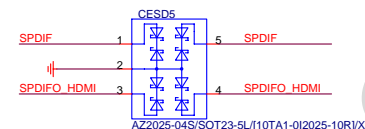
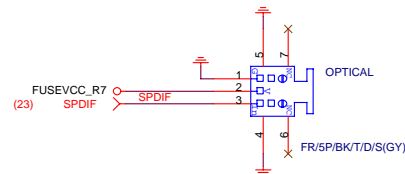
1 means floating
0 means PD 1K

Title			BIOS	
Size	Document Number	GA-Z68XP-UD3P		Rev
Custom				1.3
Date:	Tuesday, July 19, 2011	Sheet	22	of 44

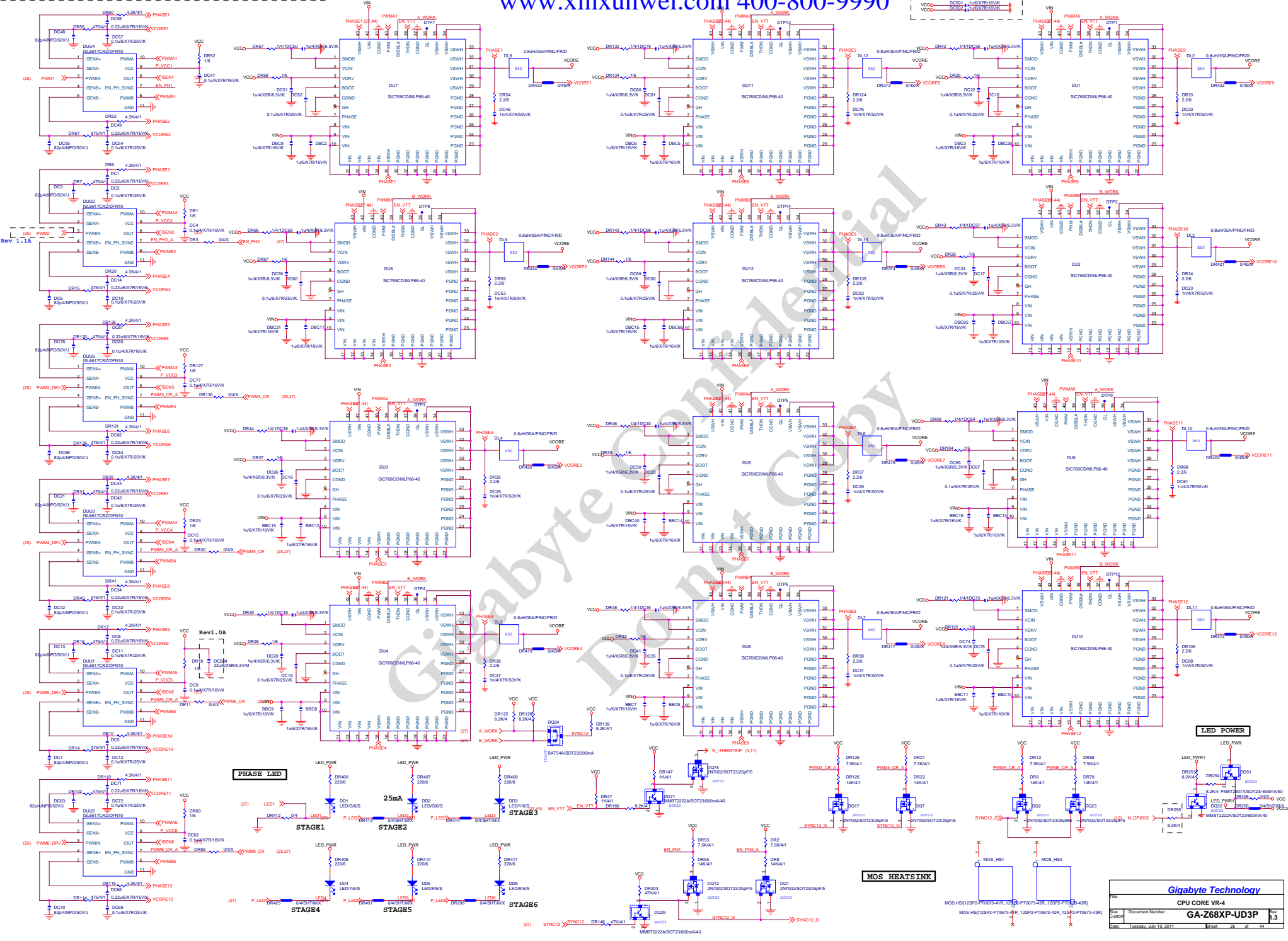


50 歐姆: 4





Digital Area



LED POWER

MOS HEATSINK

Gigabyte Technology		
CPU CORE VR-4		
GA-Z68XP-UD3P		
Doc. Number	GA-Z68XP-UD3P	1.3
Date	Tuesday, July 19, 2011	Page 26 of 34

D

D

C

C

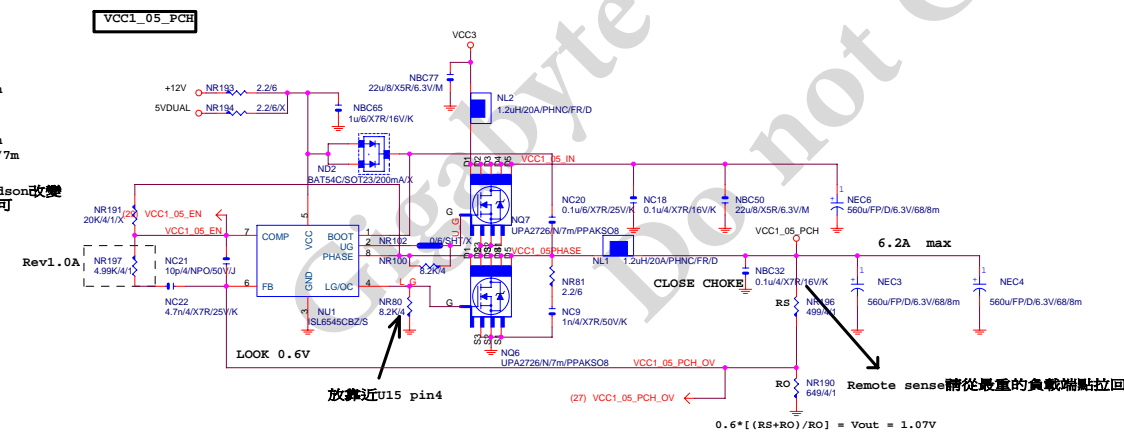
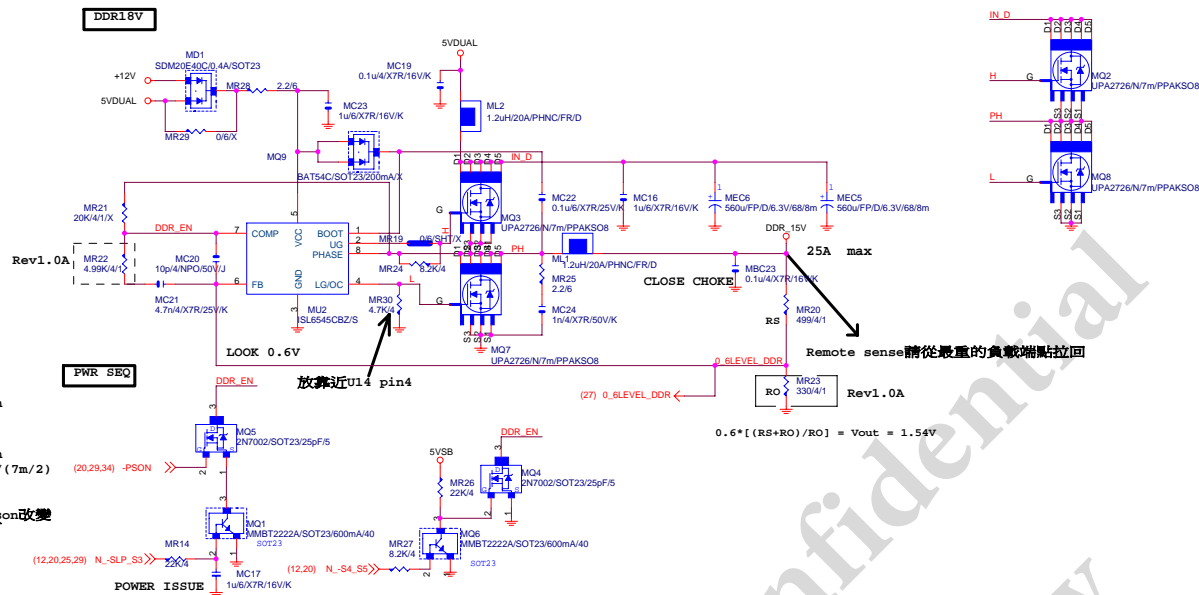
B

B

A

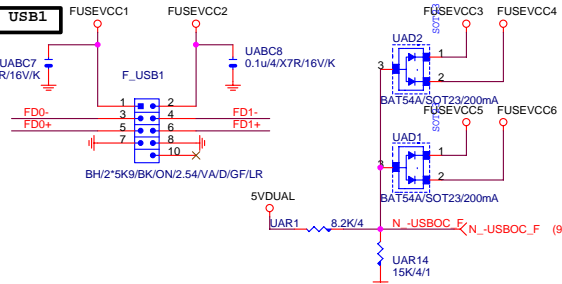
A

GIGABYTE™			
Title VCORE PHASE GEAR 4			
Size	Document Number		Rev
Custom	GA-Z68XP-UD3P		1.3
Date:	Tuesday, July 19, 2011	Sheet 28 of 44	





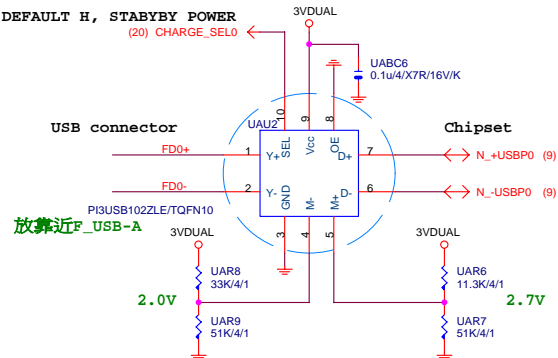
FRONT USB1



i_phone charger circuit

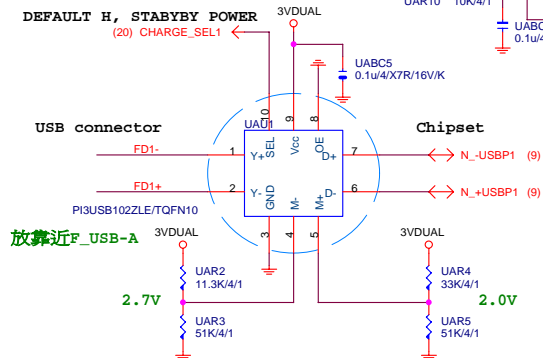
DEFAULT H, STABBY POWER

(20) CHARGE_SEL0

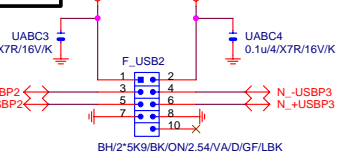


DEFAULT H, STABBY POWER

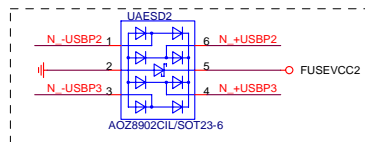
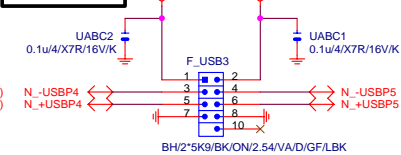
(20) CHARGE_SEL1



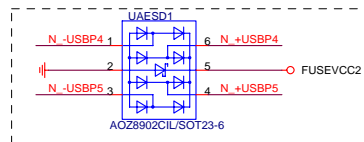
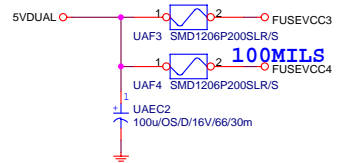
FRONT USB2



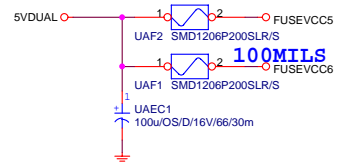
FRONT USB3



Close to connector

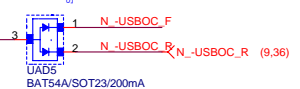


Close to connector

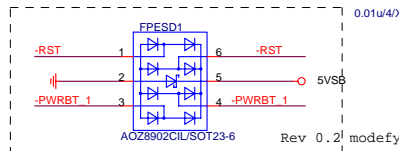


F_USB POWER PROTECT

(12) N_GPIO11



INTEL FRONT PANEL



Rev 0.2 modify

CASE OPEN

(12,13) N_RTCVDD

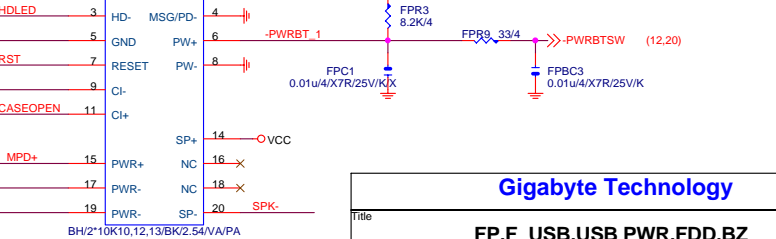
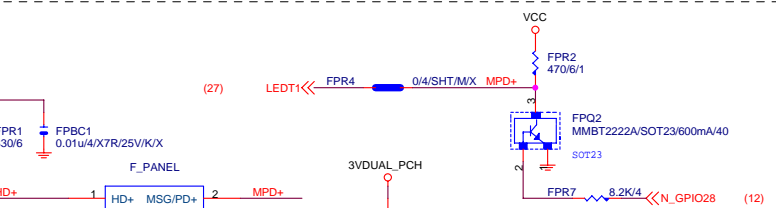
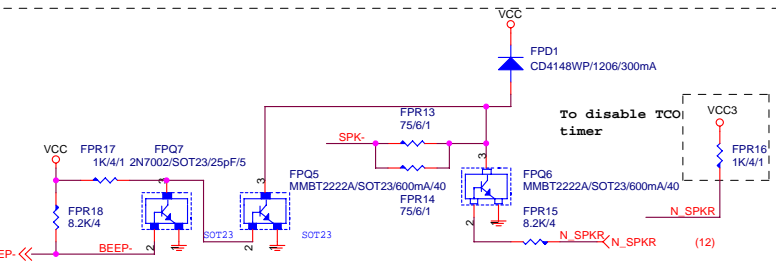
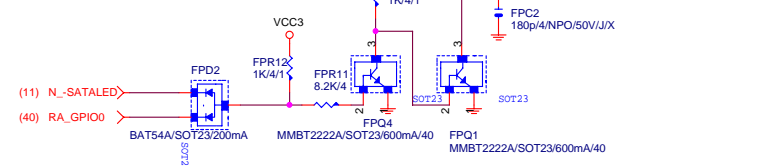
FPR8 1M/4

-CASEOPEN

-CASEOPEN (20)

FPBC4 0.01u/4/X7R/25V/K

SATA LED

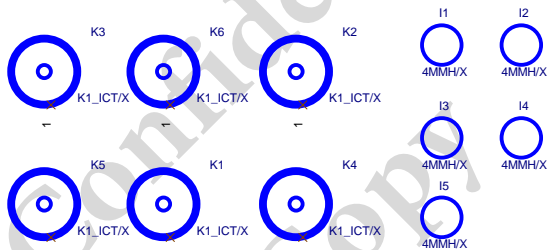
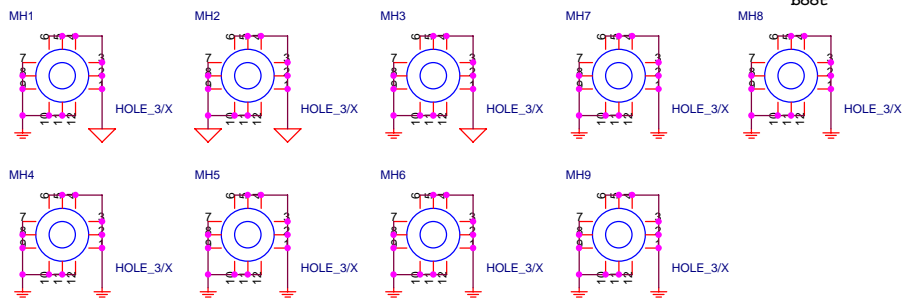
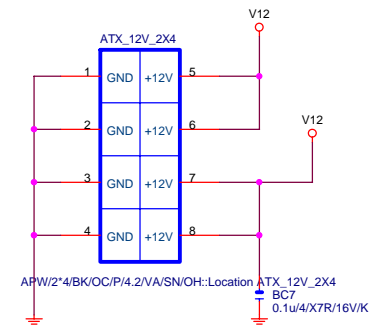
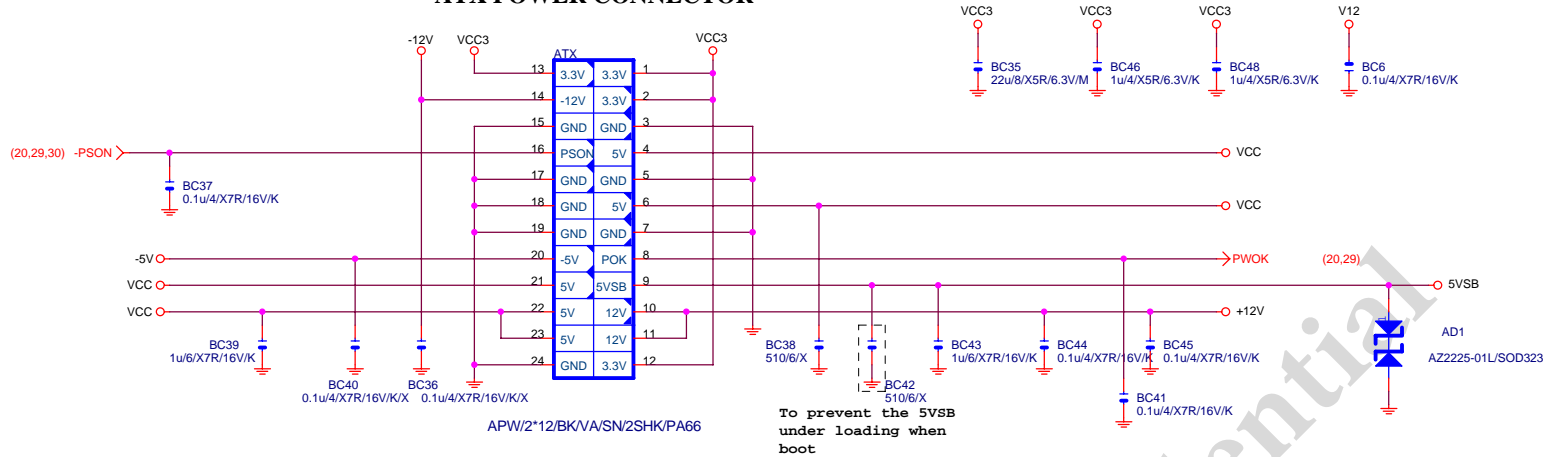


Gigabyte Technology

Title		FF,P_USB,USB PWR,FDD,BZ	
Size		GA-Z68XP-UD3P	
Date		Tuesday, July 19, 2011	
Sheet		33 of 44	

ATX POWER CONNECTOR

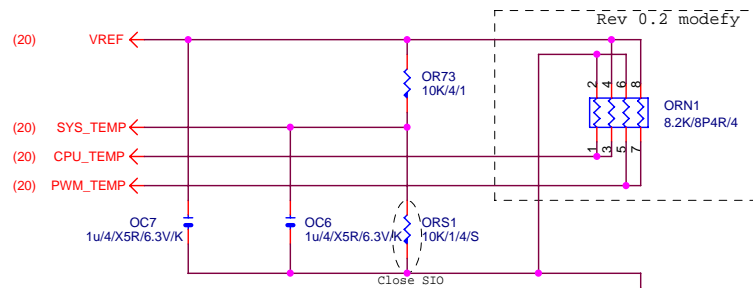
www.xinxunwei.com 400-800-9990



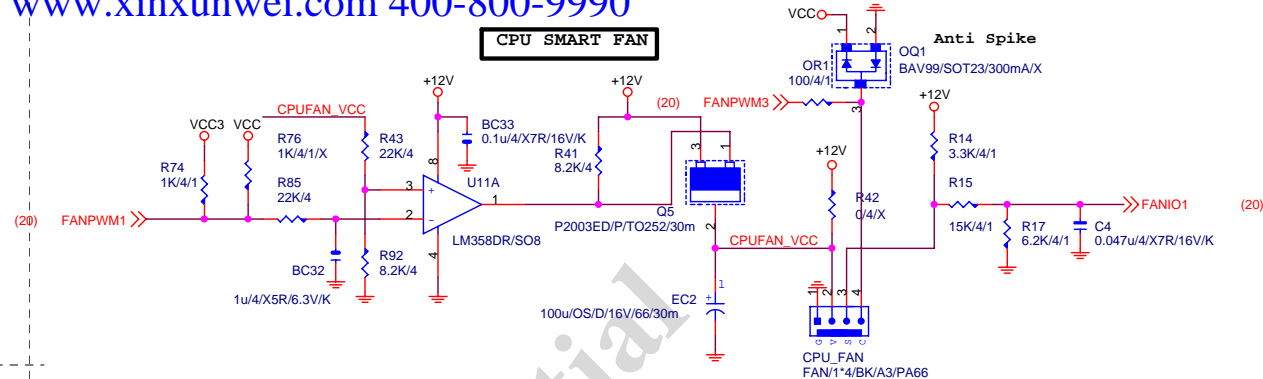
Gigabyte Technology

Title			
ATX POWER CONNECTOR			
Size	Document Number	Rev	
Custom	GA-Z68XP-UD3P	1.3	
Date:	Tuesday, July 19, 2011	Sheet	34 of 44

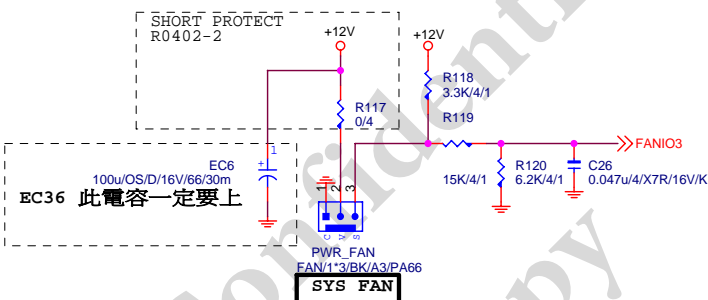
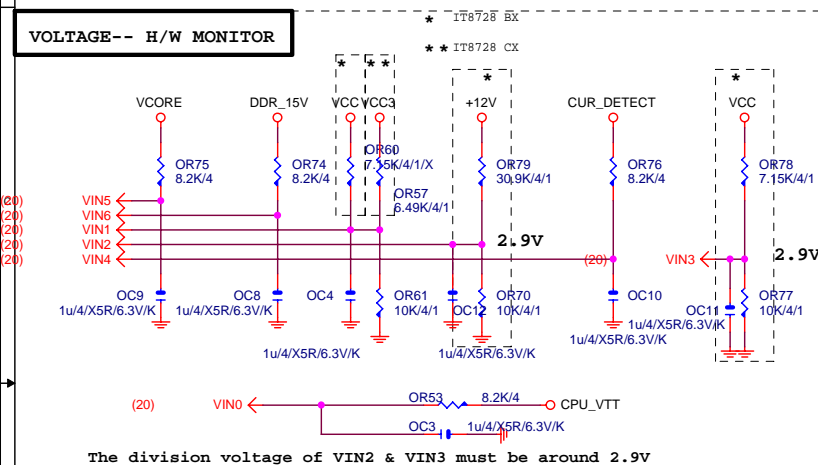
TEMP H/W MONITOR



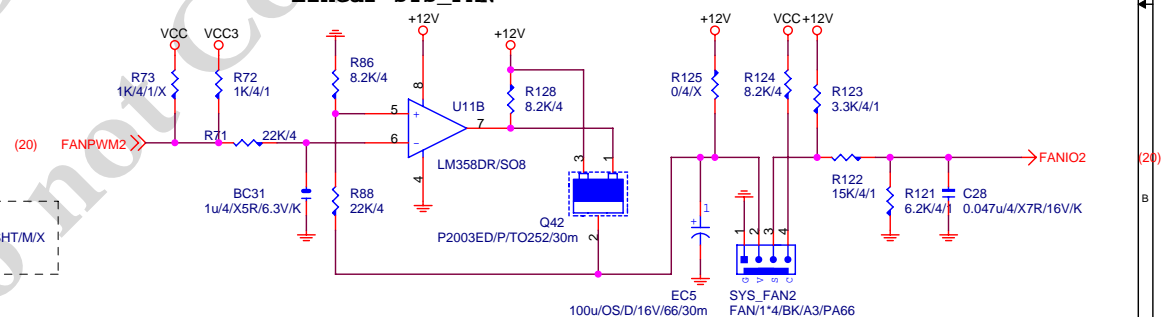
CPU SMART FAN



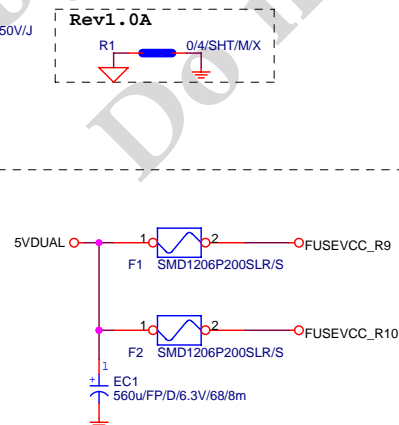
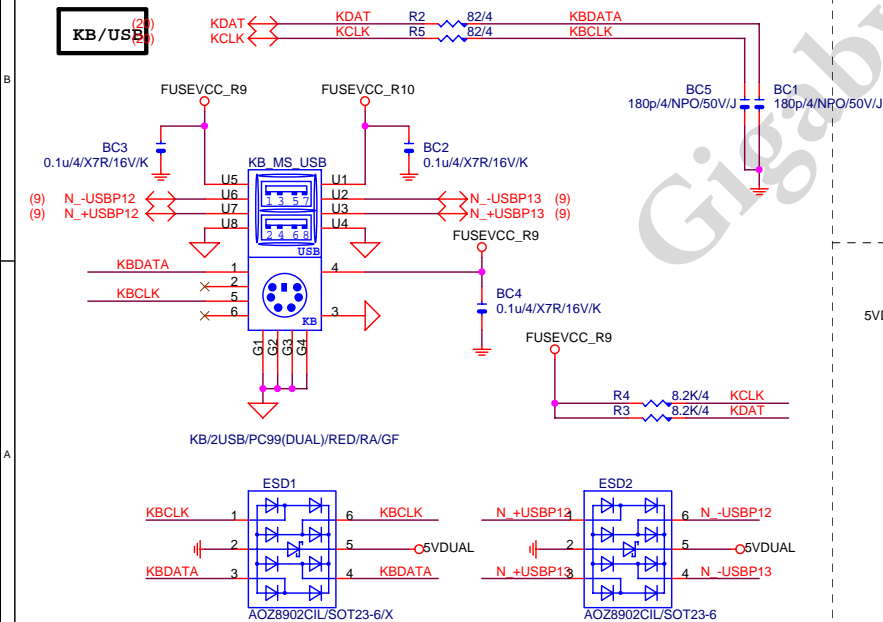
VOLTAGE-- H/W MONITOR



Linear SYS_FAN



KB/USB



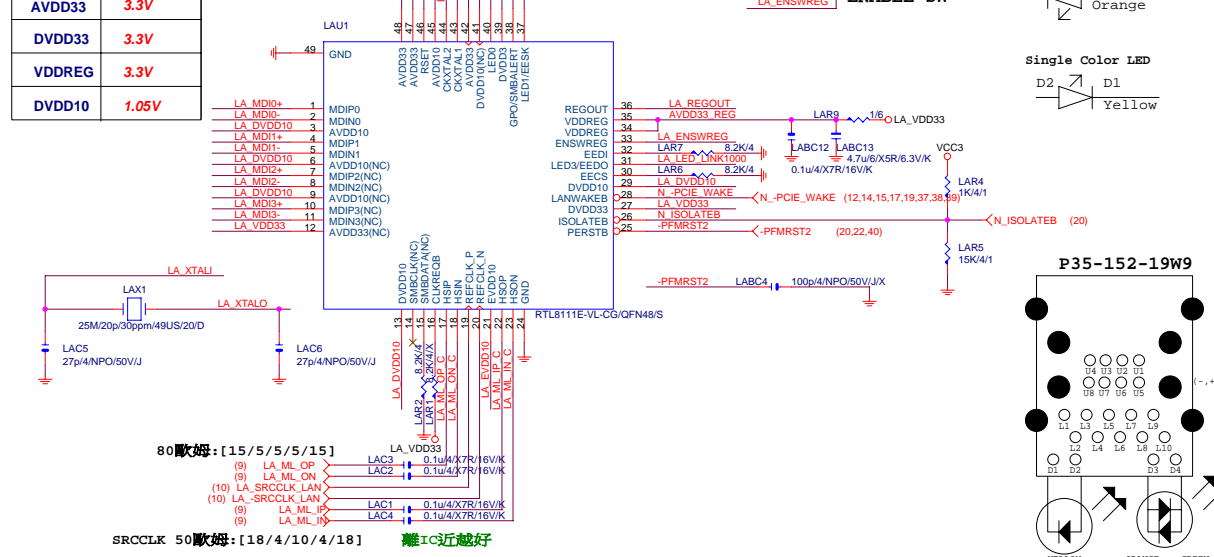
Gigabyte Technology

Title		
HWM,KB/MS, FAN CTRL		
Size	Document Number	Rev
Custom	GA-Z68XP-UD3P	1.3
Date:	Tuesday, July 19, 2011	Sheet 35 of 44

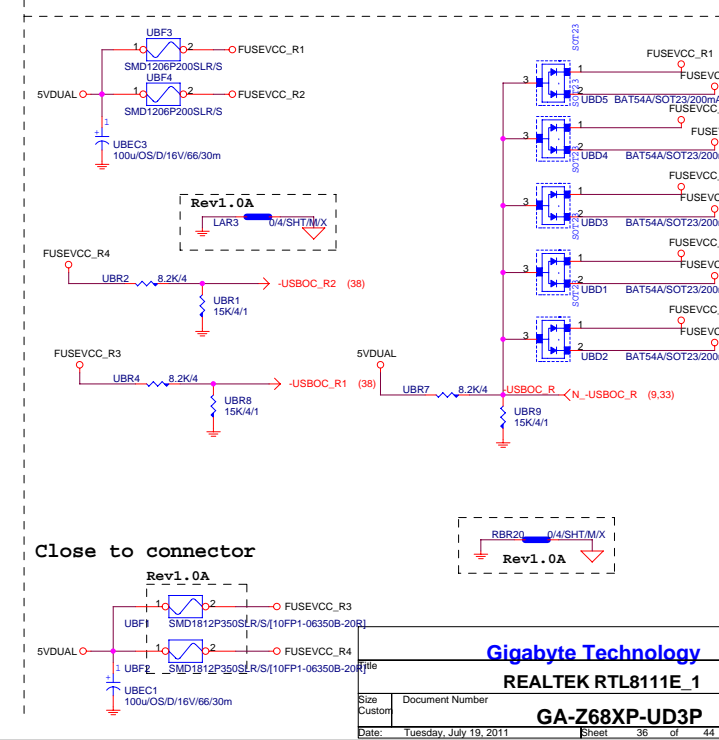
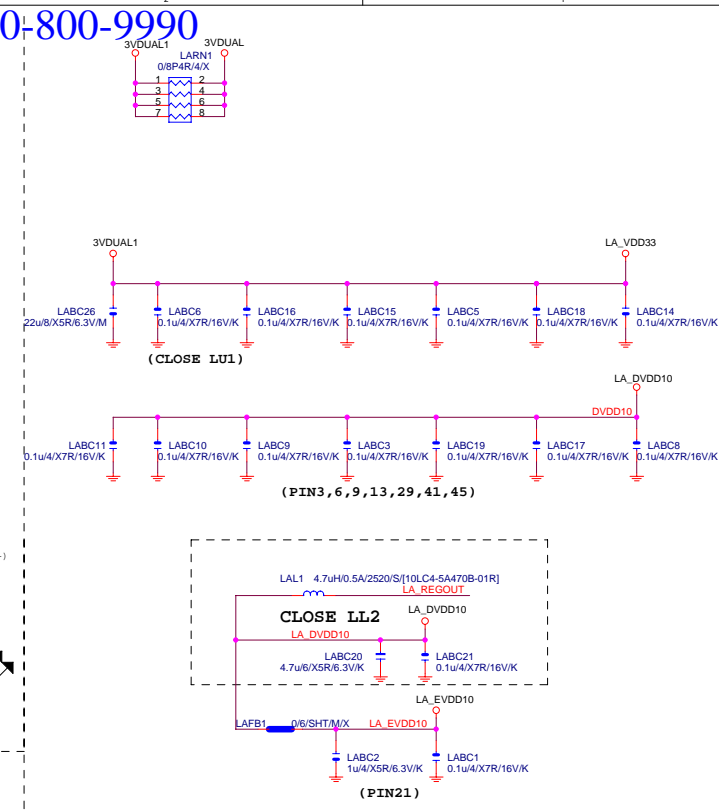
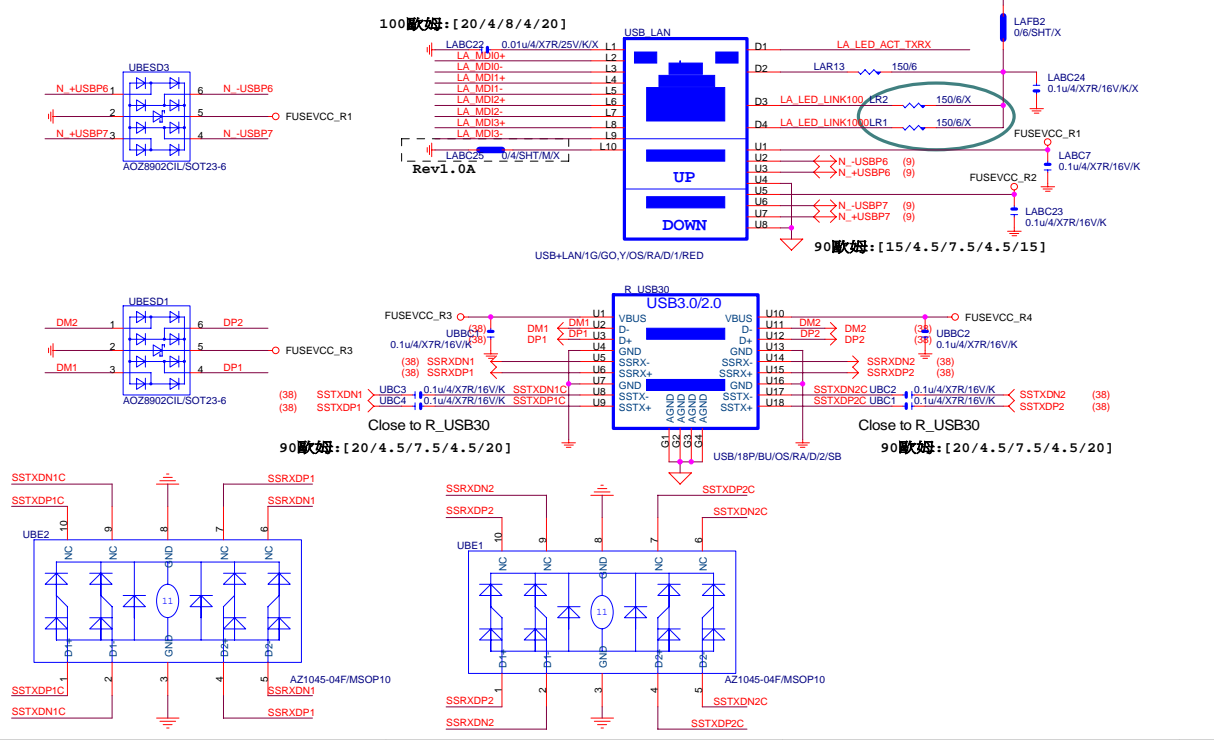
PCIE-1G LAN

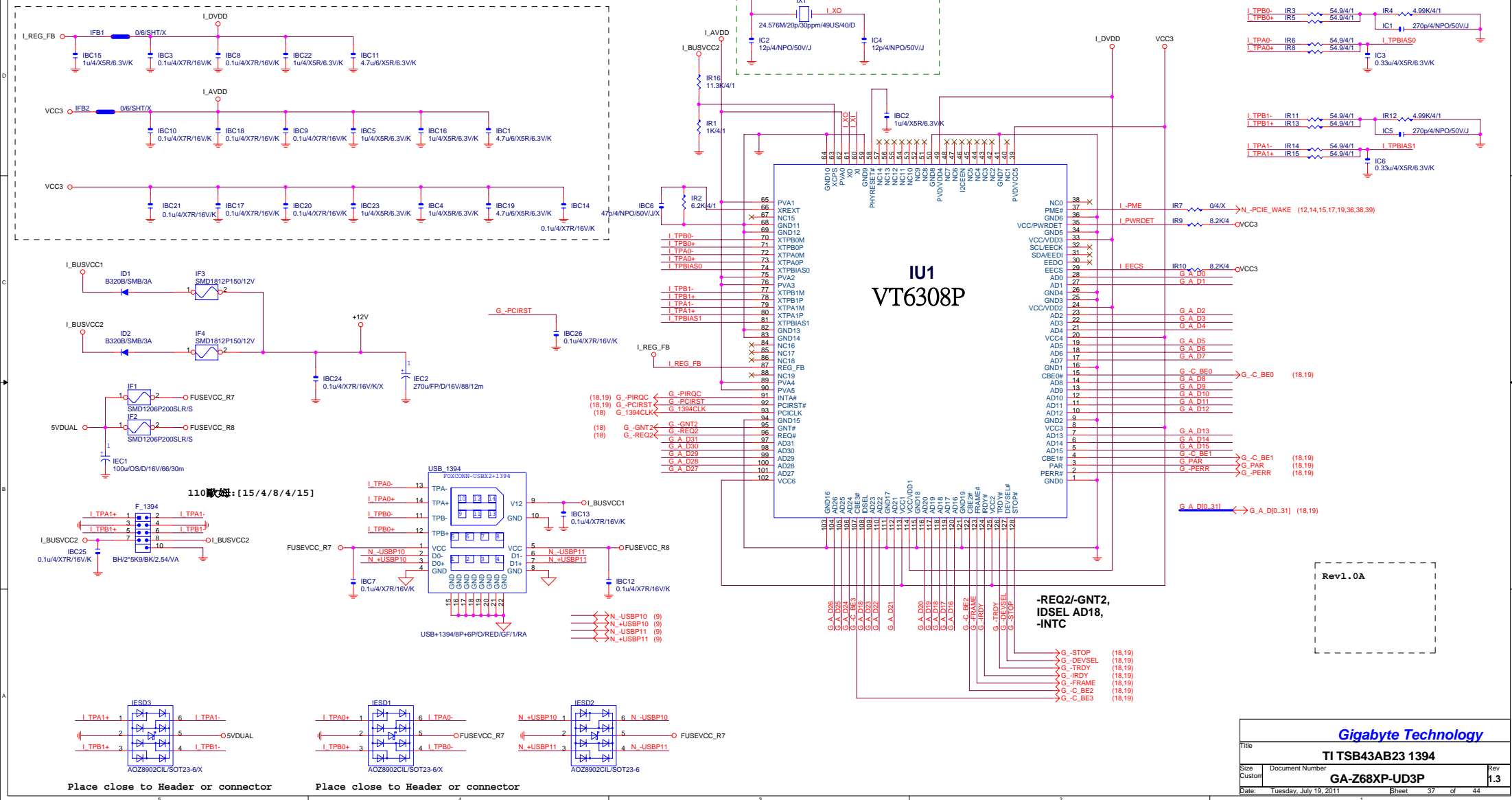
Power domain chart

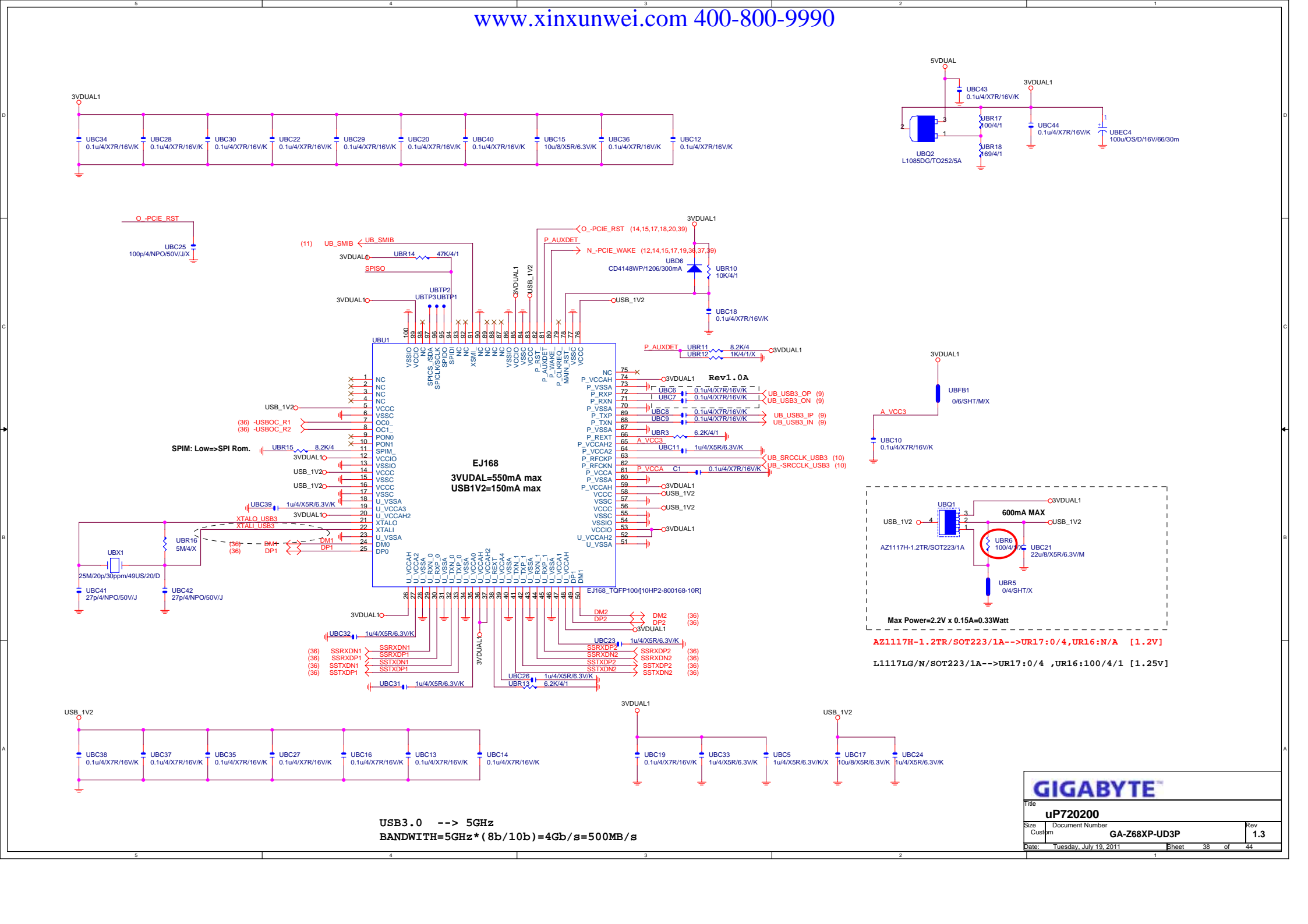
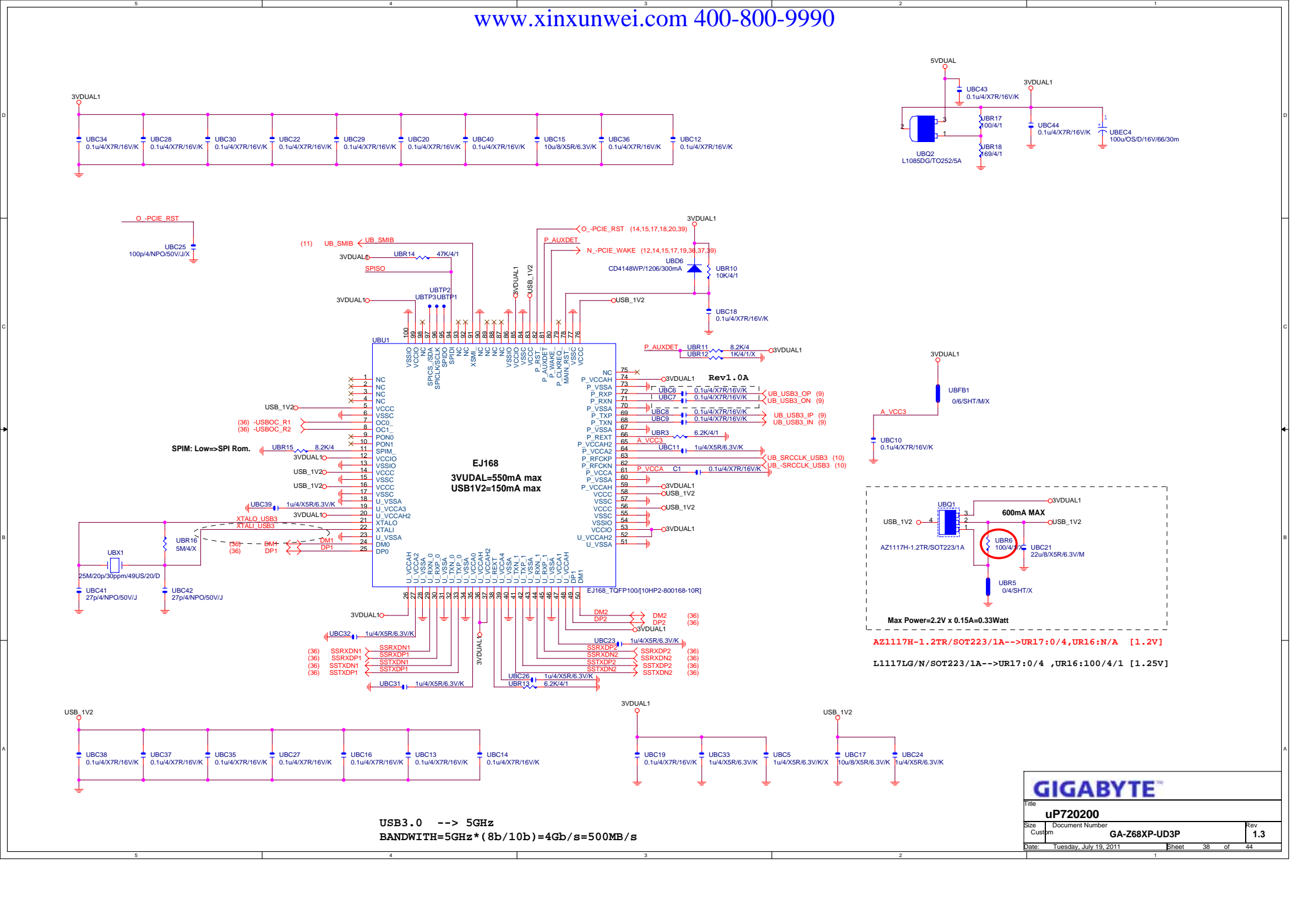
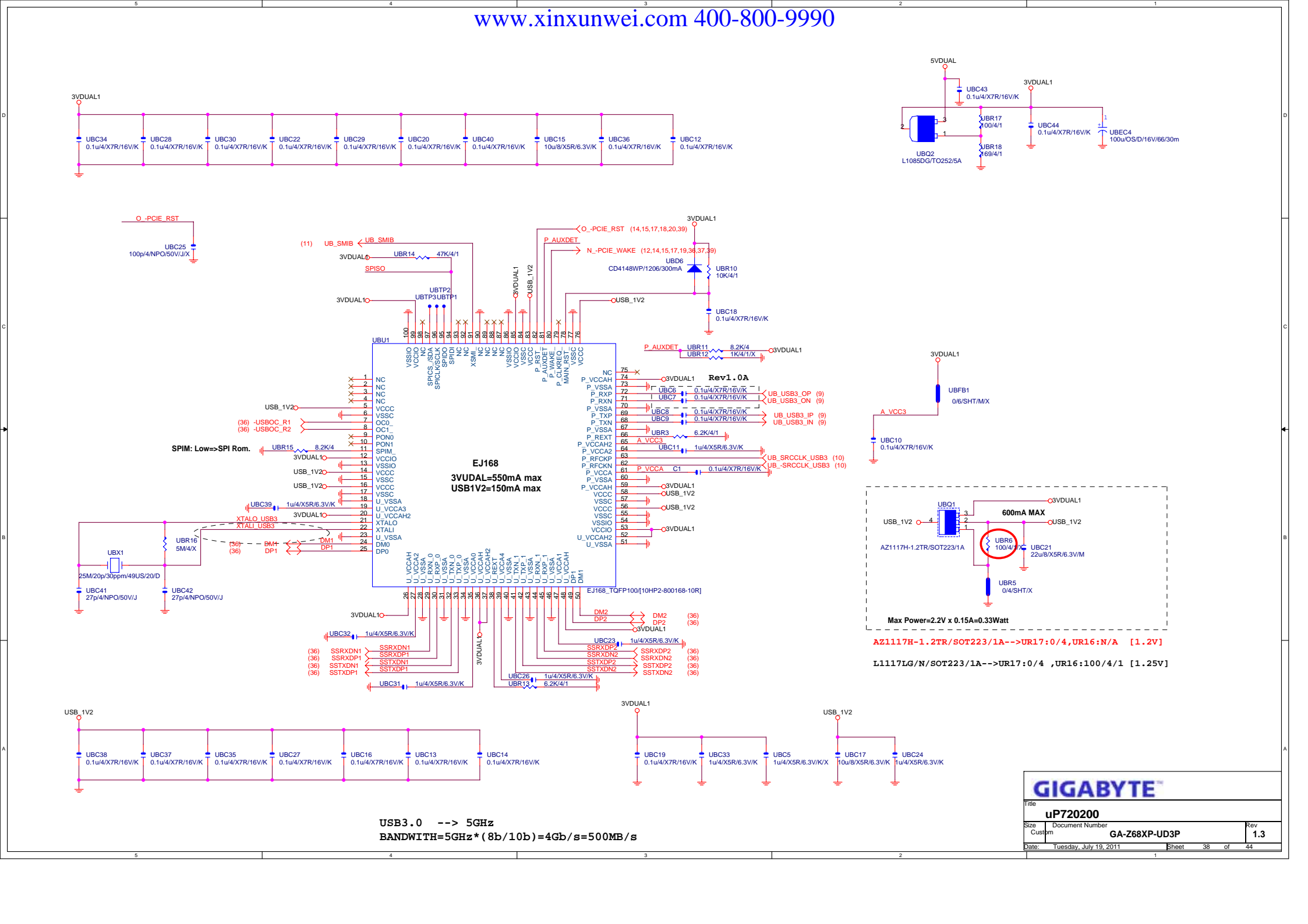
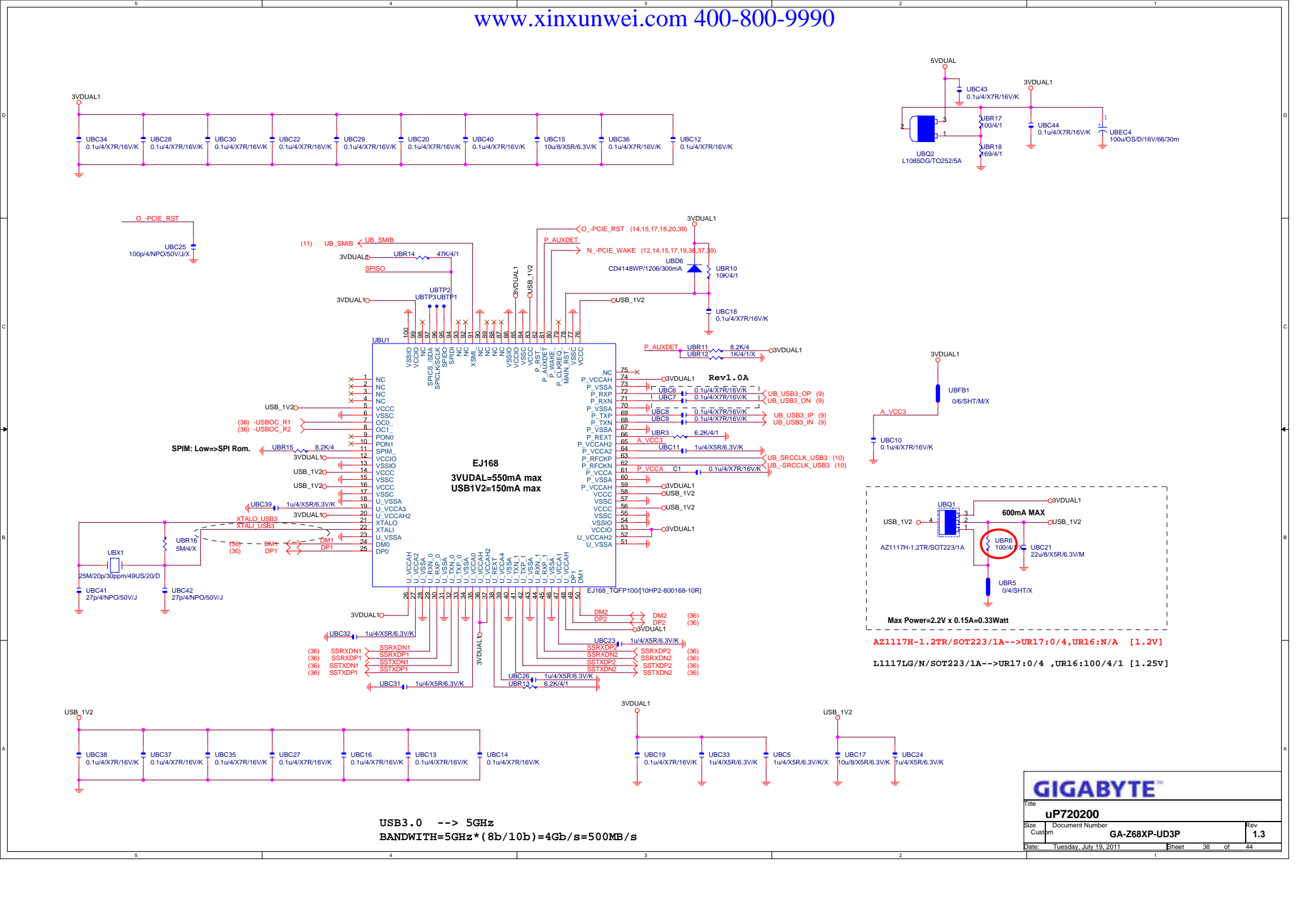
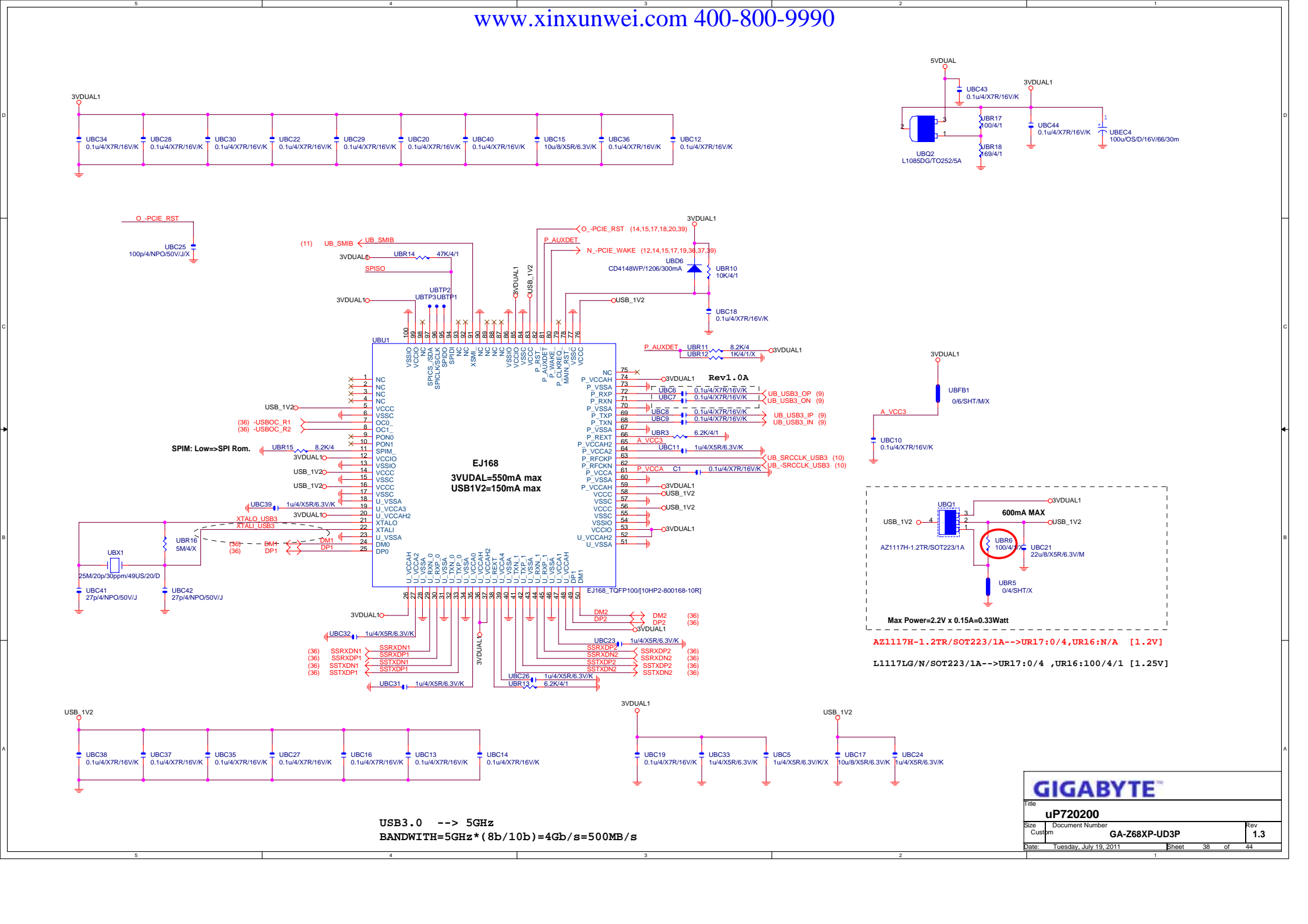
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

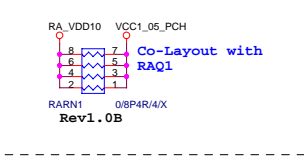
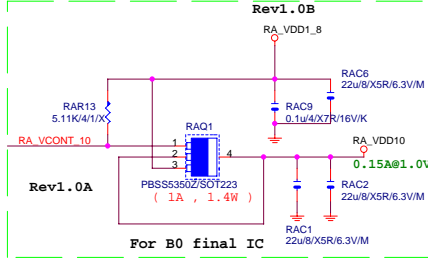
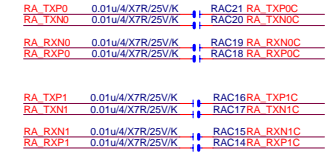
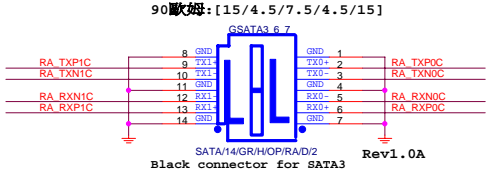
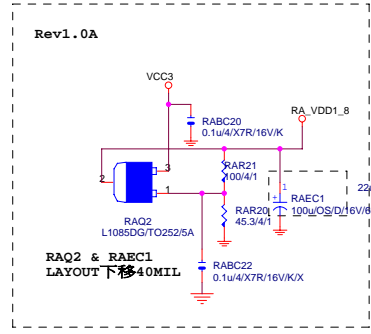
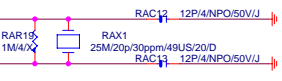
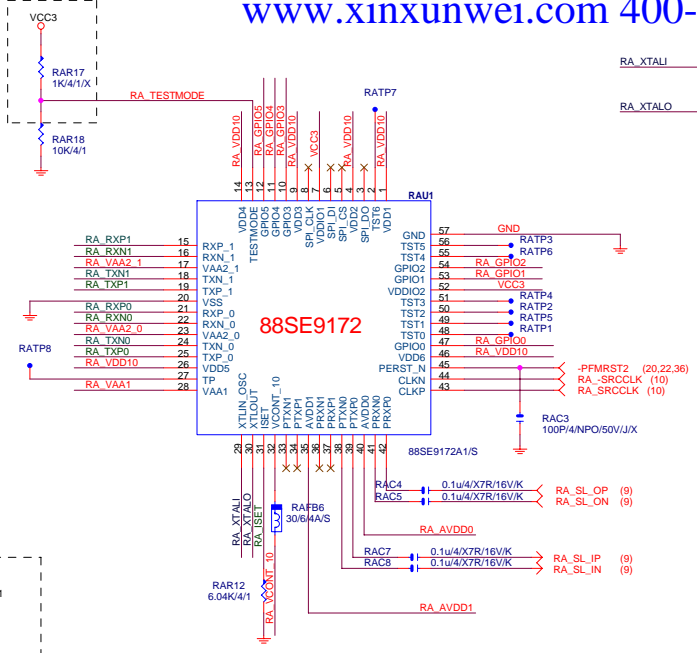
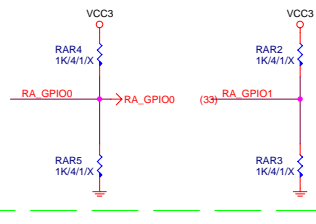
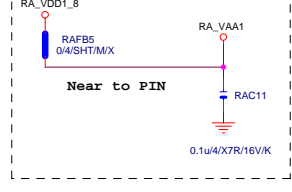
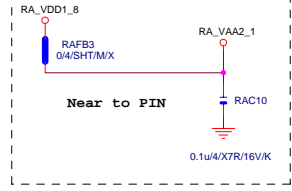
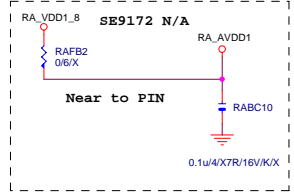
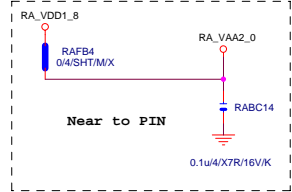
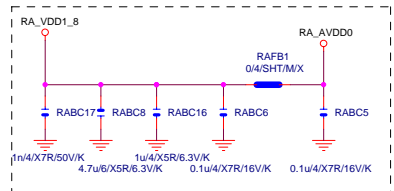
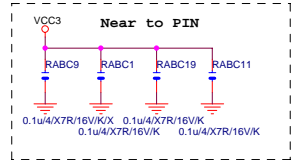
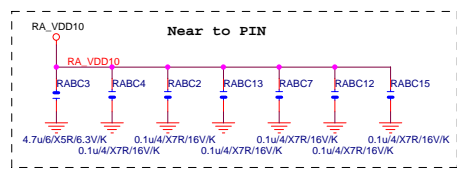


USB30_LAN CONNECTOR









Gigabyte Technology			
Title		Marvell 9172	
Size	Document Number		Rev
Custom	GA-Z68XP-UD3P		1.3
Date:	Tuesday, July 19, 2011	Sheet	41 of 44

Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

The diagram illustrates a 2D mesh network topology. It features a central square labeled **CPU**. To its left is a square labeled **PCH**. To the right of the CPU is a vertical column of four squares, each representing a router. The top router is labeled **VTT** and **VCORE**. The three routers below it are each labeled with two node IDs: the first router has **PH1** and **PH2** on the left and **PH3** and **PH4** on the right; the second router has **L4** and **L3** on the left and **DL8** and **DL6** on the right; the third router has **DL2** and **DL4** on the left and **DL9** and **DL7** on the right; and the bottom router has **DL3** and **DL5** on the left and **PH5** and **PH7** on the right. The nodes are arranged in a grid, with the CPU and PCH connected to the top router, and the routers connected to each other in a vertical chain.

散熱模組料號:

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

Gigabyte Technology			
Title			
TABLE LIST			
Size C	Document Number		Rev
	GA-Z68XP-UD3P		1.3
Date:	Tuesday, July 10, 2011	Sheet	42 of 44

